SEQUENTIAL CIRCUITS

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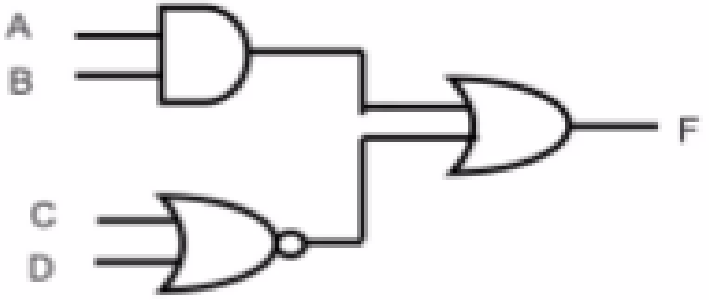
- **Combinational**
  - The output variables are dependent only on the present input values
  - It uses only logic gates
  - They are faster
  - They are simple and easy to design.
  - Example: Adder etc.
- **Sequential**
  - The outputs depend on the present input as well as past output values
  - Slower than combinational circuit.
  - It uses logic gates and storage elements
  - Harder to design
  - Example Counters etc.

Combinational vs Sequential Circuit

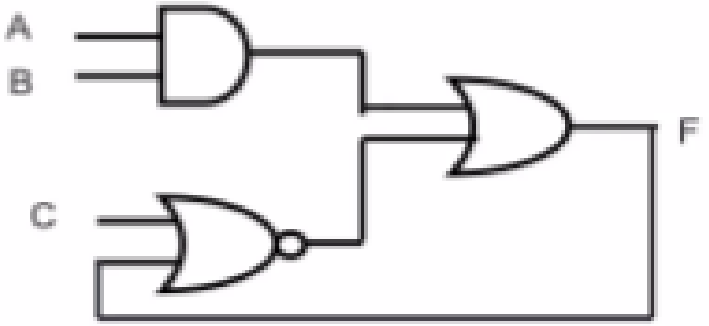
Combinational Circuit

- output determined solely by inputs



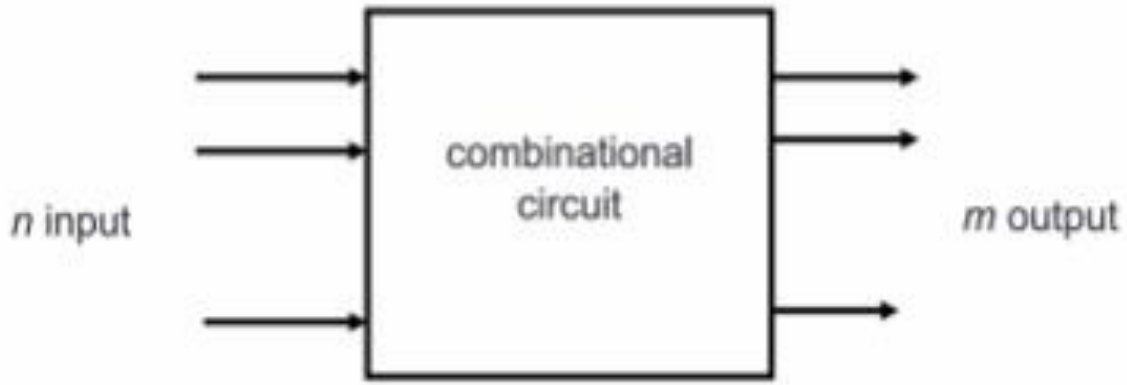
Sequential Circuit

- output determined by inputs AND previous outputs



Combinational Circuit

- Combinational Logic circuit contains logic gates where its output is determined by the combination of the current input, regardless of the output or the prior combination of input.

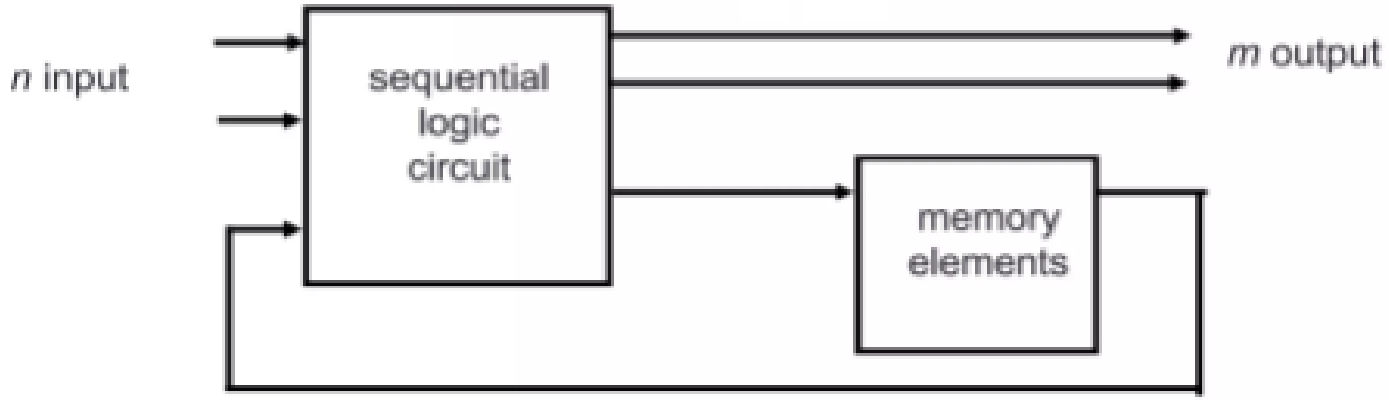


Sequential Logic

Sequential circuit consists of combinational logic circuit to which memory elements are connected to form a feedback path.

Memory elements are devices capable of storing binary information within them.

The binary information stored in the memory elements at any given time defines the state of the sequential circuits.



Sequential Circuit Types

- **Synchronous**
  - Circuit output changes only at some discrete instants of time.
  - The circuits achieves synchronization by using a timing signal called as the *clock*.
  - A clock is used for synchronization
    - ✓ Memory elements are affected only with the arrival of a clock pulse
    - ✓ If memory elements use clock pulses in their inputs, the circuit is called
      - Clocked sequential circuit (FlipFlops)
  - The status of memory element is effected only at the active edge of the clock, if input is changed.
  - Slower because of clocking.

Sequential Circuit Types

- **Asynchronous**
  - Circuit output can change at any time (clock less).
  - Unclocked latch is used as a memory element.
  - Faster because of no clock.
  - Status of memory element is changed at any time as soon as input is changed.

Clock

- It emits a series of pulses with a precise pulse width and precise interval between consecutive pulses
- Timing interval between the corresponding edges of two consecutive pulses is known as the clock cycle time, or period

Combinational Circuits	Sequential Circuits
Outputs depend only on present inputs.	Outputs depend on both present inputs and present state.
Feedback path is not present.	Feedback path is present.
Memory elements are not required.	Memory elements are required.
Clock signal is not required.	Clock signal is required.
Easy to design.	Difficult to design.

bistable devices

Two categories of bistable devices are the latch and the flip-flop. Bistable devices have two stable states, called SET and RESET; they can retain either of these states indefinitely, making them useful as storage devices. The basic difference between latches and flip-flops is the way in which they are changed from one state to the other. The flip-flop is a basic building block for counters, registers, and other sequential control logic and is used in certain types of memories.

4.0 Flip Flop (Sequential Circuits)

- What is Flip flop?

Answer:

- In digital circuits, the **flip-flop**, is a kind of **bistable multivibrator**.
- It is a Sequential Circuits / an electronic circuit which has two stable states and thereby is capable of serving as one bit of memory , bit 1 or bit 0.

There are basically 4 types of flip-flops in digital electronics:

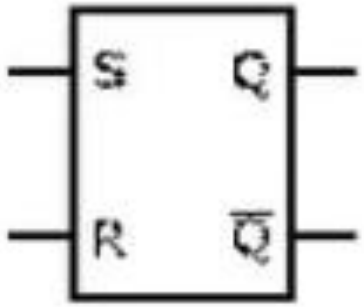
1.SR Flip-Flop
2.JK Flip-Flop
3.D Flip-Flop
4.T Flip-Flop

4.1 SR Flip Flop

- The most basic Flip Flop is called **SR Flip Flop**.
- The basic RS flip flop is an asynchronous device.
- In asynchronous device, the outputs is immediately changed anytime one or more of the inputs change just as in combinational logic circuits.
- It does not operate in step with a clock or timing.
- These basic Flip Flop circuit can be constructed using two NAND gates latch or two NOR gates latch.
- **SR Flip Flop Active Low** = NAND gates
- **SR Flip Flop Active High** = NOR gates

4.1 SR Flip Flop

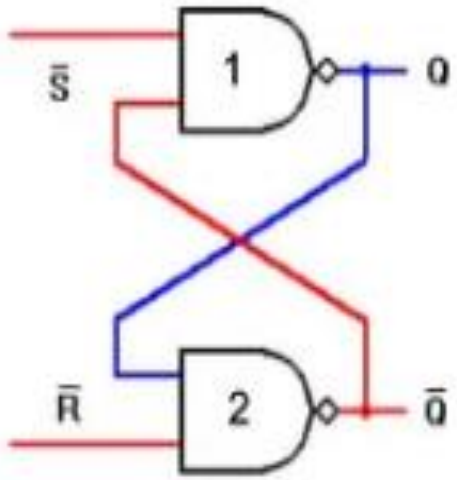
- **Figure 4.1.1:**
- **SR Flip Flop logic Symbol**



- The SR Flip Flop has two inputs, SET (S) and RESET (R).
- The SR Flip Flop has two outputs, Q and $\overline{Q}$
- The Q output is considered the normal output and is the one most used.
- The other output $\overline{Q}$ is simply the compliment of output Q.

4.1 SR Flip Flop - **NAND GATE LATCH**

- **NAND GATE LATCH**

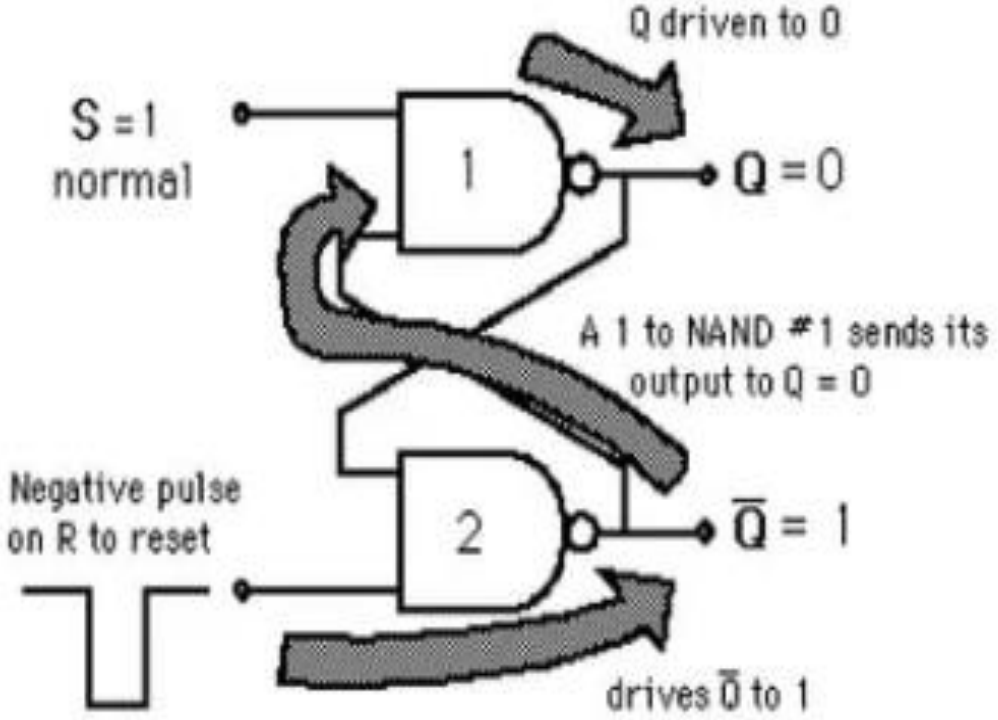


- **Figure 4.1.2: SR NAND (Active LOW) Logic circuit.**

- The NAND gate version has two inputs, SET (S) and RESET (R).
- Two outputs, Q as normal output and $\bar{Q}$ as inverted output and feedback mechanism.
- The feedback mechanism is required to form a sequential circuit by connecting the **output** of **NAND-1** to the **input** of **NAND-2** and vice versa.
- The circuit outputs depends on the inputs and also on the outputs.

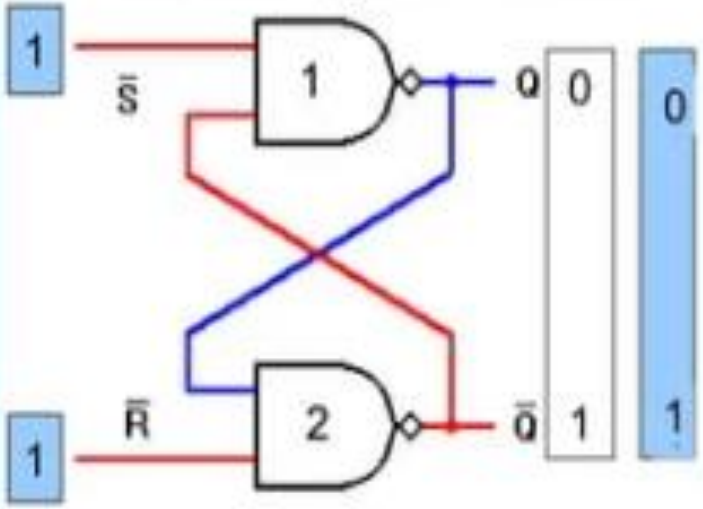
4.1 SR Flip Flop - **NAND GATE LATCH**

- Figure 4.1.3 Feedback Mechanism



4.1SR Flip Flop - **NAND GATE LATCH**

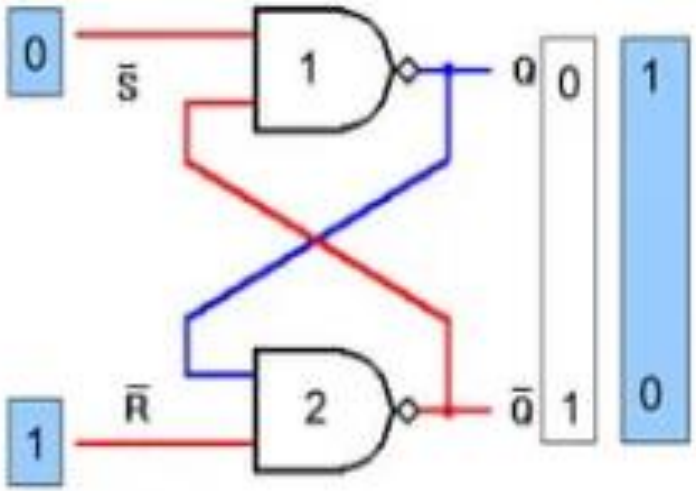
- Normal Resting State Figure 4.1.4.a



- Input S=1 , R=1 ,
- This is the normal resting state of the circuit and it has no effect of the output states.
- Output Q and $\bar{Q}$ will remain in whatever state they were in prior to the occurrence of this input condition.
- It works in **HOLD** mode of operation.

4.1 SR Flip Flop - **NAND GATE LATCH**

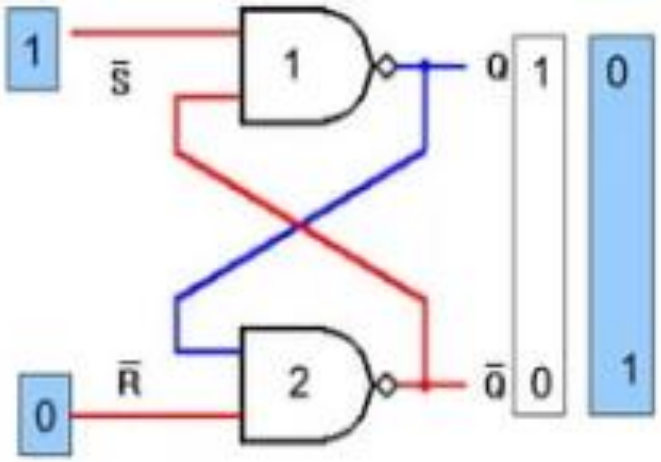
- Figure 4.1.4.b



- Input, **S = 0, R = 1**
- This will set **Q = 1.**
- It works in **SET** mode operation.

4.1 SR Flip Flop - **NAND GATE LATCH**

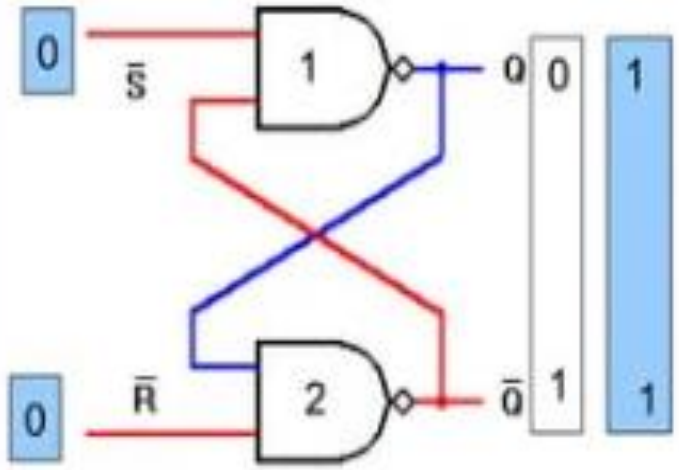
- Figure 4.1.4.c



- Input **S = 1, R = 0**
- This will reset **Q = 0.**
- It works in **RESET** mode operation.

4.1 SR Flip Flop - **NAND GATE LATCH**

- Figure 4.1.4.d



- This condition tries to set and reset the NAND gate latch at the same time.
- It produces $Q = \bar{Q} = 1$
- This is unexpected condition, since the two outputs should be inverses of each other.
- If the inputs are returned to 1 simultaneously, the output states are unpredictable.
- This input condition should not be used and when circuits are constructed, the **design** should make this condition

  S = R = 0 **never** arises.

It is called **INVALID/PROHIBITED**

4.1 SR Flip Flop - **NAND GATE LATCH**

- From the description of the NAND gate latch operation, it shows that the SET and RESET inputs are active LOW.
- The SET input will set Q = 1 when SET is 0 (LOW).RESET input will reset Q = 0 when RESET is 0 (LOW)
- In the prohibited/INVALID state both outputs are 1. This condition is not used on the RS flip-flop. The set condition means setting the output Q to 1.
- Likewise, the reset condition means resetting (clearing) the output Q to 0. The last row shows the disabled, or *hold*, condition of the RS flip-flop. The outputs remain as they were before the hold condition existed. There is no change in the outputs from the previous states.

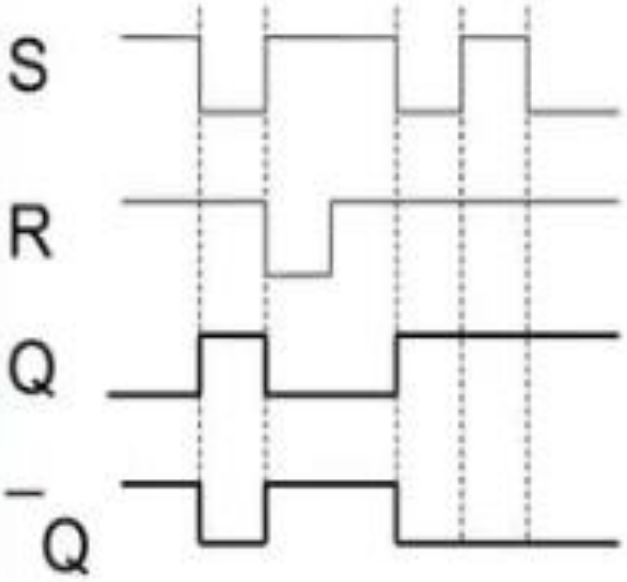
The flip-flop *memorizes* the previous condition.

- **Figure 4.1.5 : SR NAND gate latch Truth Table**

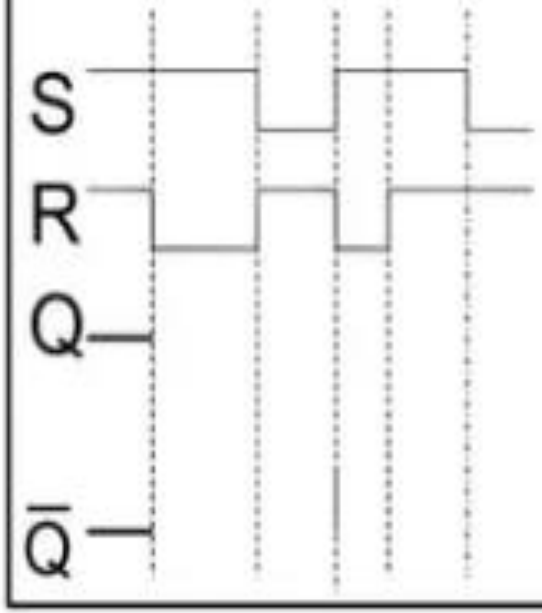
S	R	Q	$\bar{Q}$	STATUS
0	0	1	1	**INVALID**
0	1	1	0	**SET**
1	0	0	1	**RESET**
1	1	Q	$\bar{Q}$	**HOLD** (NoChange)

4.1 SR NAND Flip Flop-Waveforms

Example 4.1.1: Determine the output of NAND gate latch which Q initialy 0 for the given input waveform.

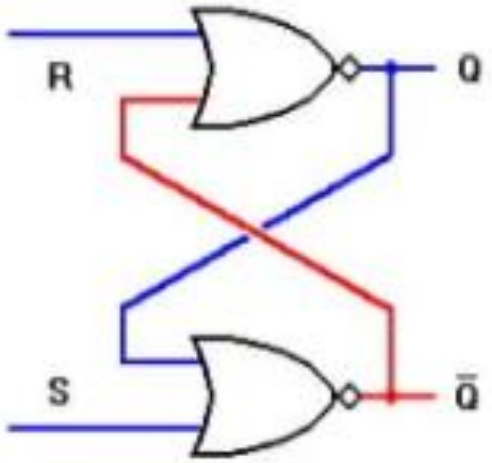


Exercise 4.1.1:
Determine the output of NAND gate latch which **Q initially 1** for the given input waveforms.



4.1 SR Flip Flop - **NOR GATE LATCH**

- **NOR GATE LATCH**

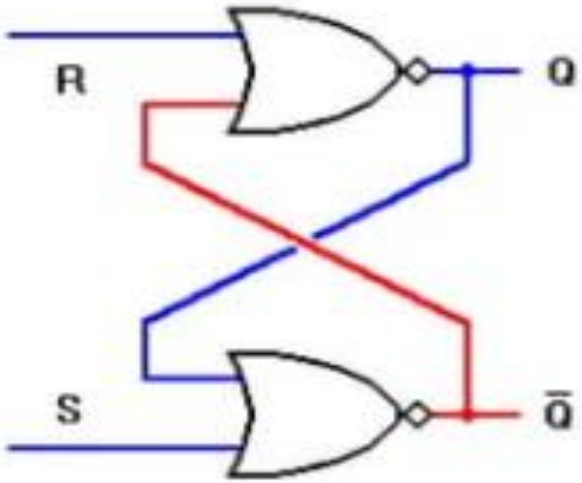


- Figure 4.1.6: **SR NOR (Active HIGH) Logic circuit**

- The latch circuit can also be constructed using two NOR gates latch.
- The construction is similar to the NAND latch except that the normal output **Q** and inverted output $\bar{\mathbf{Q}}$ have reversed positions.

4.1 SR Flip Flop - **NOR GATE LATCH**

SR FLIP FLOP NOR
(Active HIGH) Logic circuit



The analysis of a **SR FLIP FLOP NOR :**

* **S = 0, R = 0;** This is the normal resting state of the circuit and it has no effect of the output states. **Q and** $\overline{Q}$ will remain in whatever state they were in prior to the occurrence of this input condition. It works in **HOLD (no change)** mode operation.

- **S = 0, R = 1;** This will reset **Q to 0**, it works in ***RESET*** mode operation.

4.1 SR Flip Flop - **NOR GATE LATCH**

- **S = 1, R = 0;** This will set **Q to 1**, it works in **SET** mode operation.
- **S = 1, R = 1;** This condition tries to set and reset the NOR gate latch at the same time, and it produces **$Q = \overline{Q} = 0$.** This is an unexpected condition and are not used.

Since the two outputs should be inverse of each other. If the inputs are returned to 1 simultaneously, the output states are unpredictable.

This input condition should not be used and when circuits are constructed, the design should make this condition SET=RESET = 1 never arises.

4.1 SR Flip Flop - **NOR GATE LATCH**

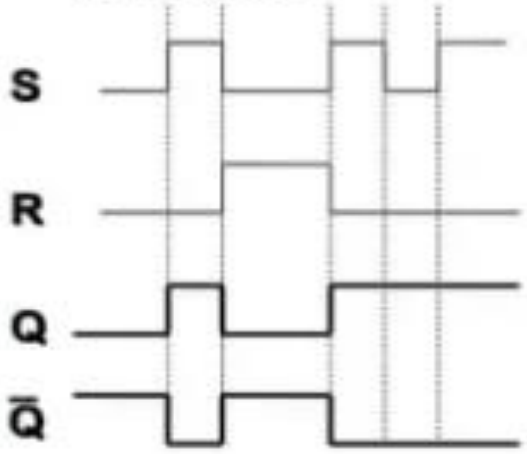
- From the description of the NOR gate latch operation, it shows that the SET and RESET inputs are Active HIGH.
- The SET input will set Q = 1 when SET is 1 (HIGH). RESET input will reset Q when RESET is 1 (HIGH).

- Figure 4.1.7 : **SR NOR gate latch Truth Table**

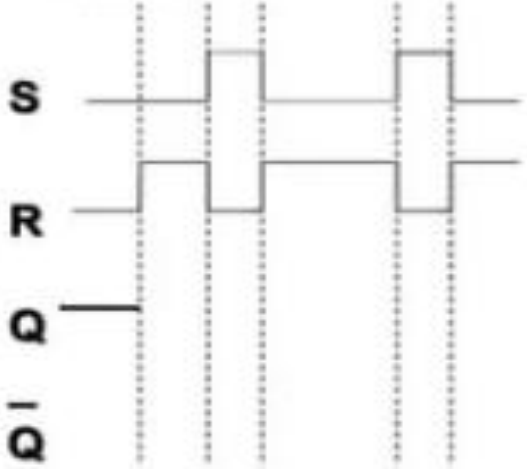
S	R	Q	$\bar{Q}$	STATUS
0	0	Q	$\bar{Q}$	HOLD (NoChange)
0	1	0	1	RESET
1	0	1	0	SET
1	1	0	0	INVALID

4.1 SR NOR Flip Flop -**Waveforms**

- **Example 4.1.2**: Determine the output of NOR gate latch which **Q initially 0** for the given input waveforms.



- **Exercise 4.1.2** : Determine the output of NOR gate latch which Q initially 1 for the given input waveforms.



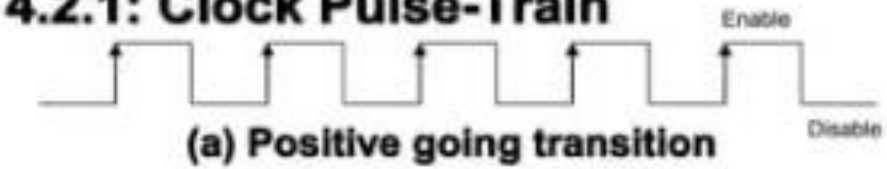
4.2 The CLOCK

- In synchronous device, the exact times at which any output can change states are controlled by a signal commonly called the clock.
- The clock signal is generally a rectangular pulse train or a square wave
- The clock is distributed to all parts of the system, and most of the system outputs can change state only when the clock makes a transition.

4.2 The CLOCK

- When the clock changes from a LOW state to a HIGH state, this is called the positive-going transition (PGT) or positive edge triggered.
- When the clock changes from a HIGH state to a LOW state, it is called negative going transition (NGT) or negative edge triggered.

Figure 4.2.1: Clock Pulse-Train



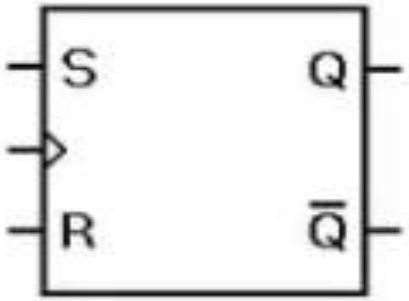
(a) Positive going transition

(b) Negative going transition

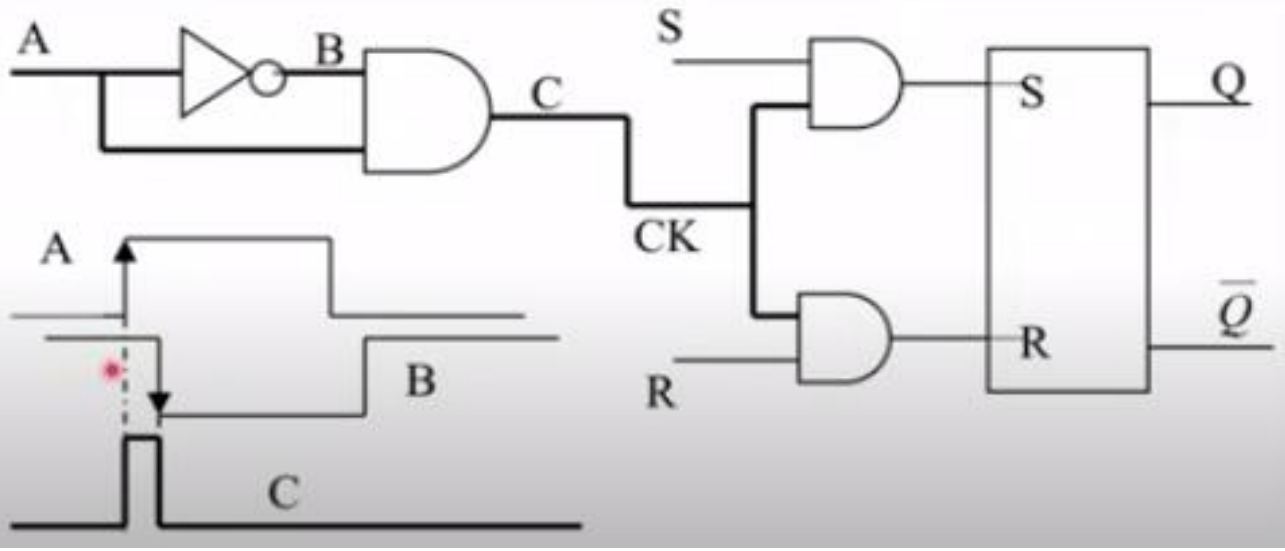
4.2 Clocked SR Flip Flop

- Additional clock input is added to change the SR flip-flop from an element used in asynchronous sequential circuits to one, which can be used in synchronous circuits.
- The clocked SR flip flop logic symbol that is triggered by the PGT is shown in **Figure 4.2.2**
- Its means that the flip flop can change the output states only when clock signal makes a transition from LOW to HIGH.

- Figure 4.2.2 : **PGT Clocked SR Flip flop symbol**



Rising Edge - حساس للجبهة الصاعدة



4.2 Clocked RS Flip Flop

Figure 4.2.3: **Truth Table for clocked SR Flip Flop**

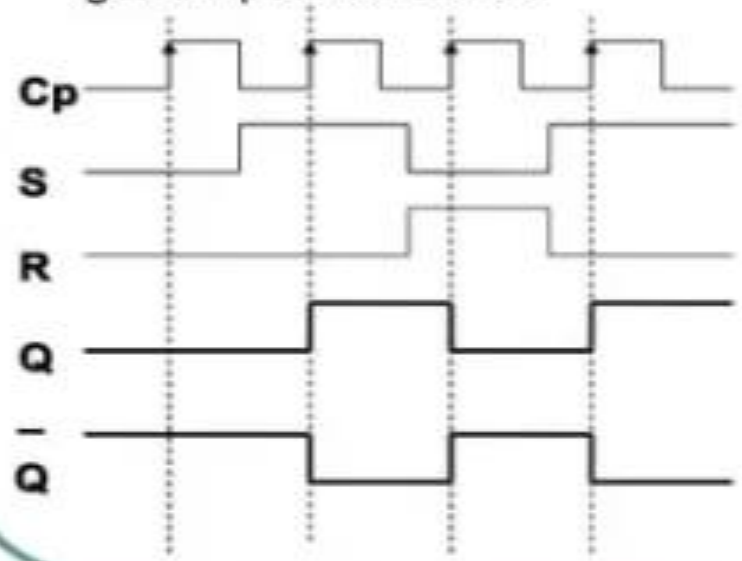
clock	S	R	Q	$\bar{Q}$	STATUS
↑	0	0	Q	$\bar{Q}$	**HOLD** (NoChange)
↑	0	1	0	1	**RESET**
↑	1	0	1	0	**SET**
↑	1	1	0	0	**INVALID**

- The **Truth Table** in figure 4.2.3 shows how the flip flop output will respond to the PGT at the clocked input for the various combinations of SR inputs and output.

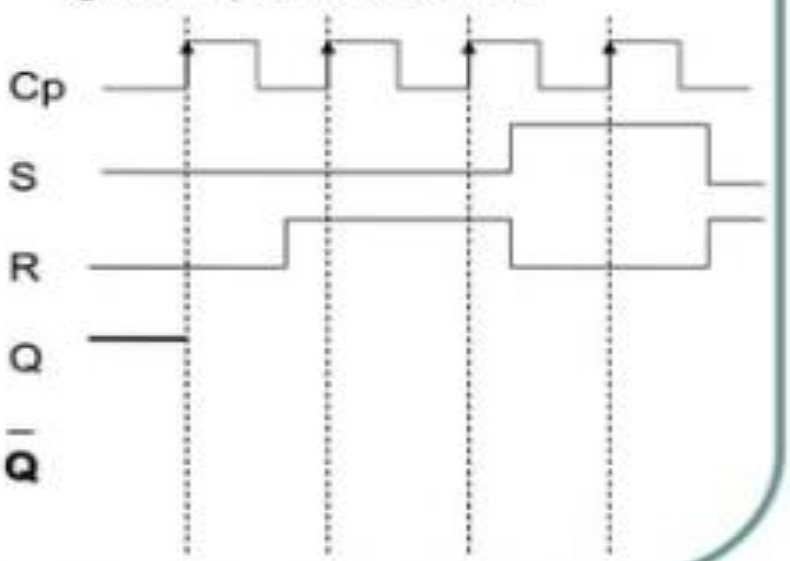
- The up arrow symbol indicates **PGT.**

4.2 Clocked SR Flip Flop

- **Example 4.2.1:** Determine the output of **PGT** clocked SR flip flop which **Q initially 0** for the given input waveforms

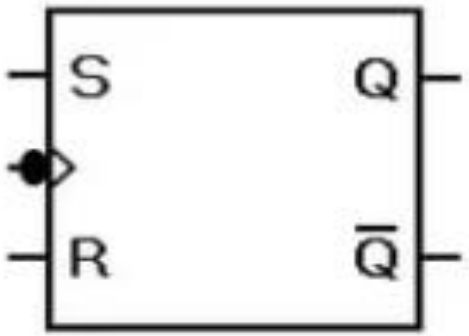


- **Exercise 4.2.1:** Determine the output of **PGT** clocked SR flip flop which **Q initially 1** for the given input waveforms.



4.2 Clocked SR Flip Flop

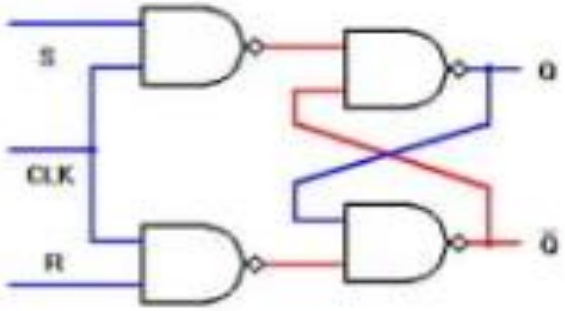
- Figure 4.2.4 : **NGT Clocked SR Flip flop symbol**



- The clocked SR Flip Flop logic symbol that is triggered by the NGT is shown in **Figure 4.2.4**
- It means that the Flip flop can change the output states only when clocked signal makes a transition from **HIGH to LOW**.

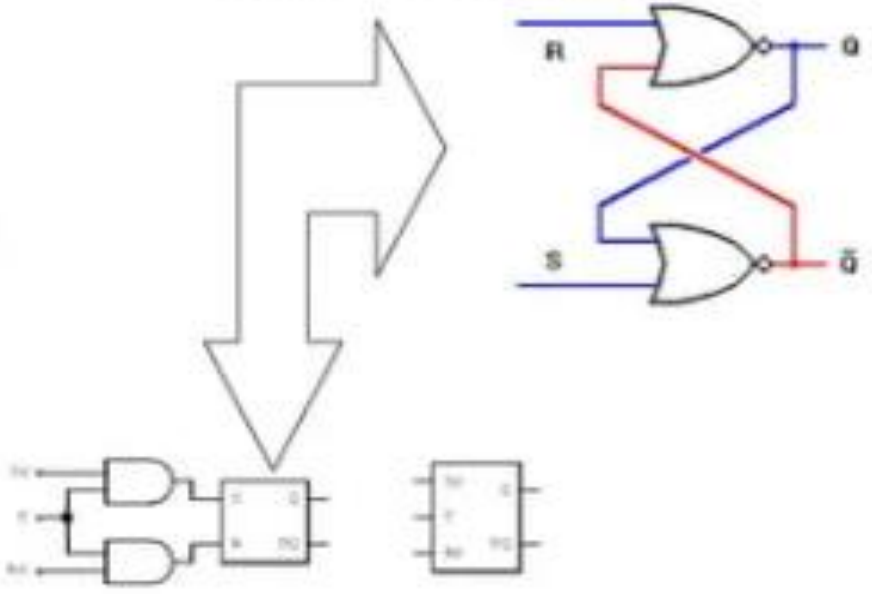
4.2 Clocked SR Flip Flop

- Figure 4.2.6: **CLOCKED SR FLIP FLOP LOGIC CIRCUIT**



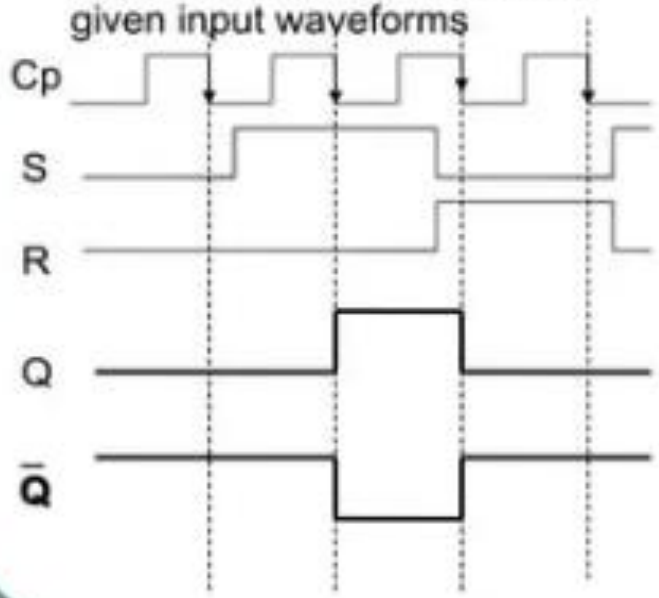
S_C	R_C	C	Q	$\bar{Q}$
x	x	0	no change	
0	0	1	no change	
0	1	1	0	1
1	0	1	1	0
1	1	1	undefined	
0	0	$\downarrow$	no change	
0	1	$\downarrow$	0	1
1	0	$\downarrow$	1	0
1	1	$\downarrow$	undefined	

- If used **NOR Gate**, must used **AND** Gate in front.

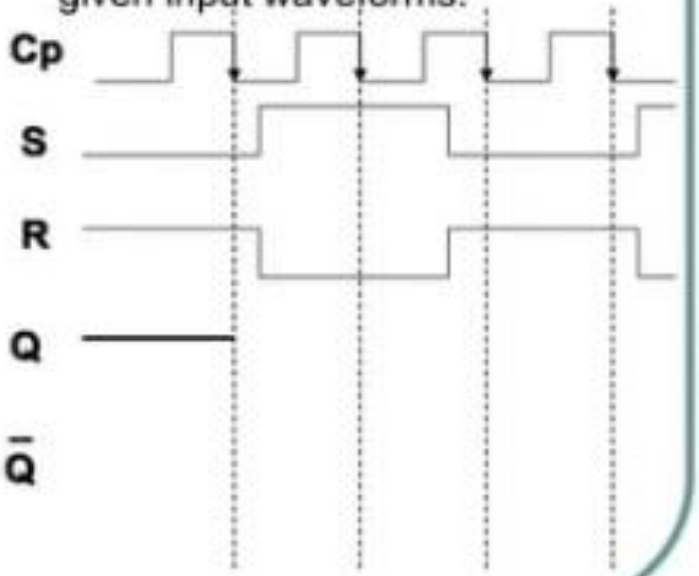


4.2 Clocked SR Flip Flop

- **Example 4.2.2**: Determine the output of **NGT** clocked SR flip flop which **Q initially 0** for the given input waveforms



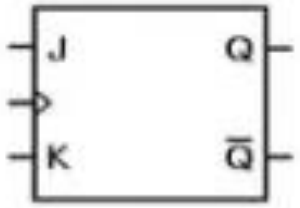
- **Exercise 4.2.2**: Determine the output of **NGT** clocked SR flip flop which **Q initially 1** for the given input waveforms.



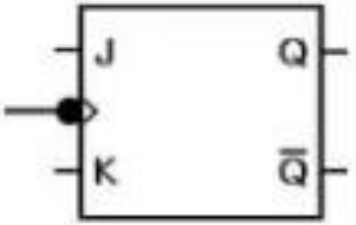
4.3 JK Flip Flop - Symbol

- Another types of Flip flop is JK flip flop.
- It differs from the RS flip flops when J=K=1 condition is not indeterminate but it is defined to give a very useful changeover (toggle) action.
- Toggle means that **Q** and $\bar{Q}$ will switch to their opposite states.
- The JK Flip flop has clock input Cp and two control inputs J and K.
- Operation of Jk Flip Flop is completely described by truth table in Figure 4.3.3.

- Figure 4.3.1 : **PGT JK Flip flop symbol**



- Figure 4.3.2 : **NGT JK Flip flop symbol**

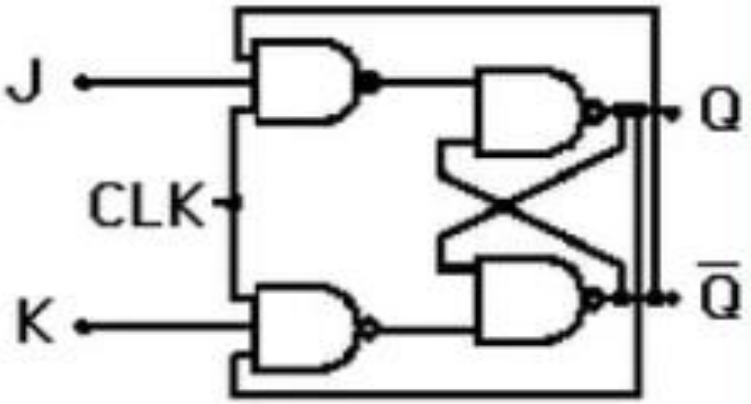


4.3 JK Flip Flop – Truth Table And Logic Circuit

Figure 4.3.3: **Truth Table for JK Flip Flop**

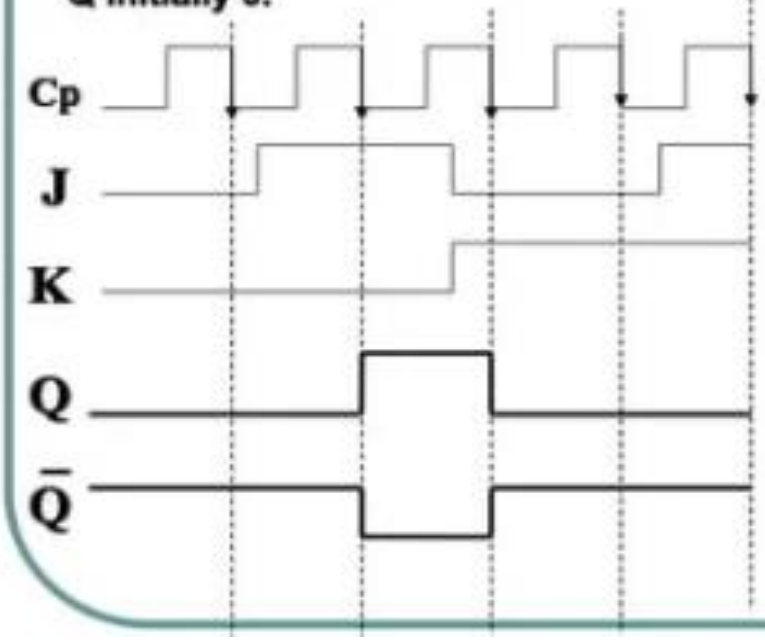
clock	J	K	Q	$\bar{Q}$	STATUS
↑	0	0	Q	$\bar{Q}$	HOLD (No Change)
↑	0	1	1	0	RESET
↑	1	0	0	1	SET
↑	1	1	$\bar{Q}$	Q	Toggle

- Figure 4.3.4: **JK FLIP FLOP LOGIC CIRCUIT**

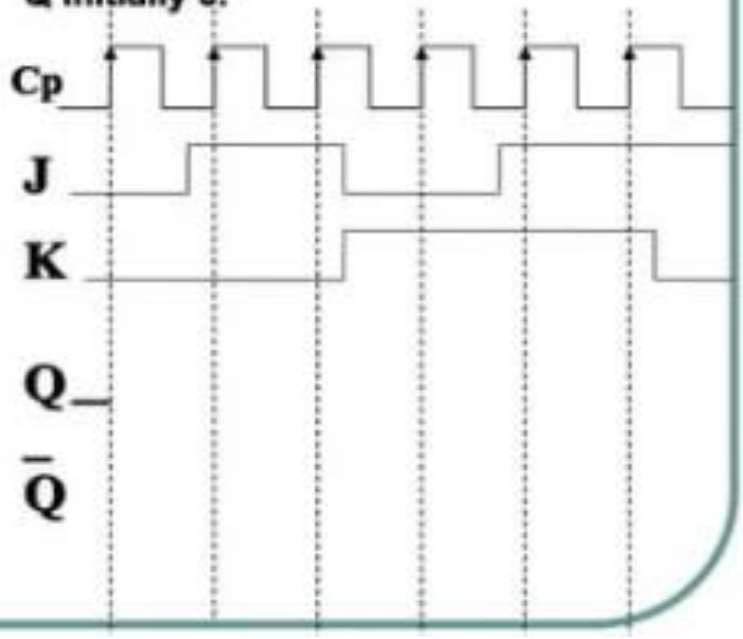


4.3 JK Flip Flop - waveforms

Exercise 4.3.1:Determine the output of **NGT** clocked JK flip flop for the given input waveforms which the **Q initially 0.**



Exercise 4.3.2:Determine the output of **PGT** clocked JK flip flop for the given input waveforms which the **Q initially 0.**



4.5 T Flip Flop - Symbol

- The T flip flop has only the Toggle and Hold Operation.
- If Toggle mode operation. The output will toggle from 1 to 0 or vice versa.

- **Figure 4.5.1:** Symbol for T Flip Flop

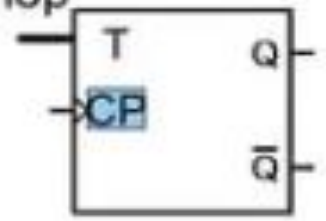
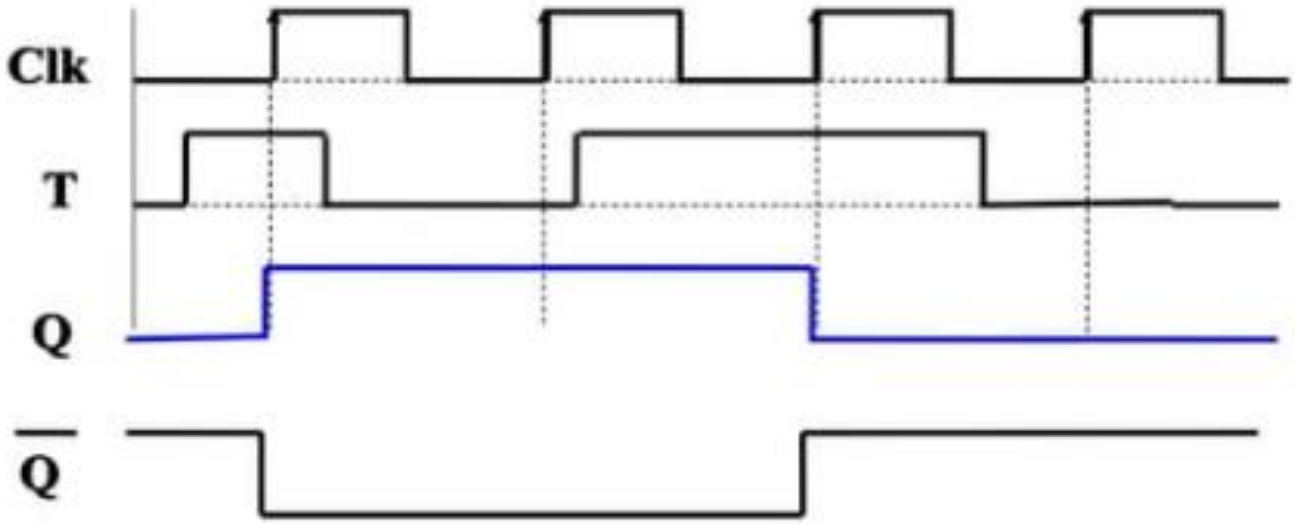


Figure 4.5.2 :Truth Table for T Flip Flop

T	clock	Q	$\bar{Q}$	status
0	↑	Q	$\bar{Q}$	HOLD
1	↑	$\bar{Q}$	Q	TOGOL

4.5 T Flip Flop – Waveforms

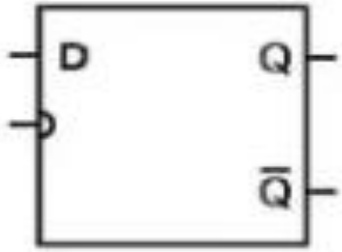
Example 4.5.1 : Determine the output of **PGT T** flip flop for the given input waveforms which the **Q initially 0.**



4.6 D Flip Flop

- Also Known as Data Flip flop
- Can be constructed from RS Flip Flop or JK Flip flop by addition of an inverter.
- Inverter is connected so that the R input is always the inverse of S (or J input is always complementary of K).
- The D flip flop will act as a storage element for a single binary digit (Bit).

- **Figure 4.6.1 :**
- **D Flip flop symbol**



4.6 D Flip Flop - Symbol

- PGT
- NGT

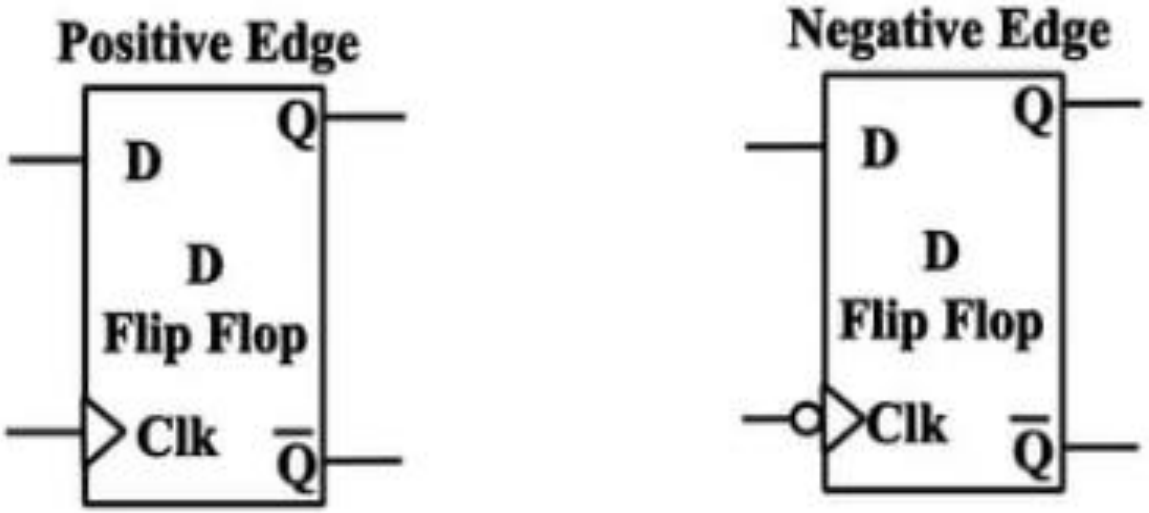
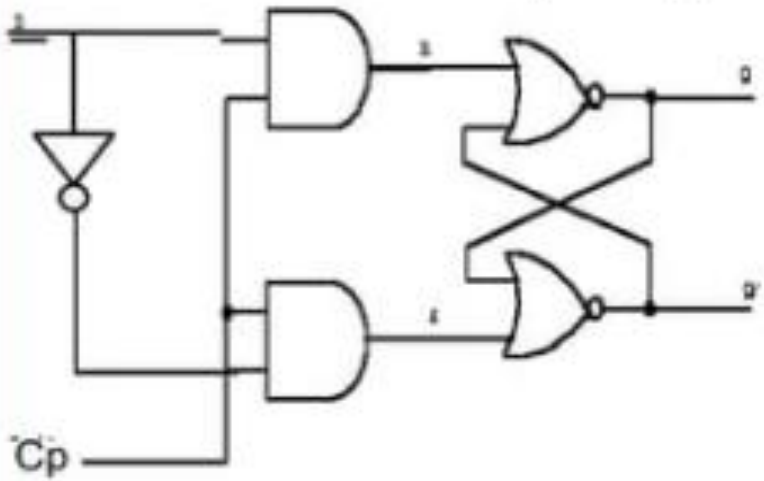


Figure 4.6.2 : D Flip flop symbol using JK Flip Flop / SR Flip Flop

4.6 D Flip Flop- Logic circuit-Truth Table

- **Figure 4.6.3:** Logic circuit for D Flip Flop

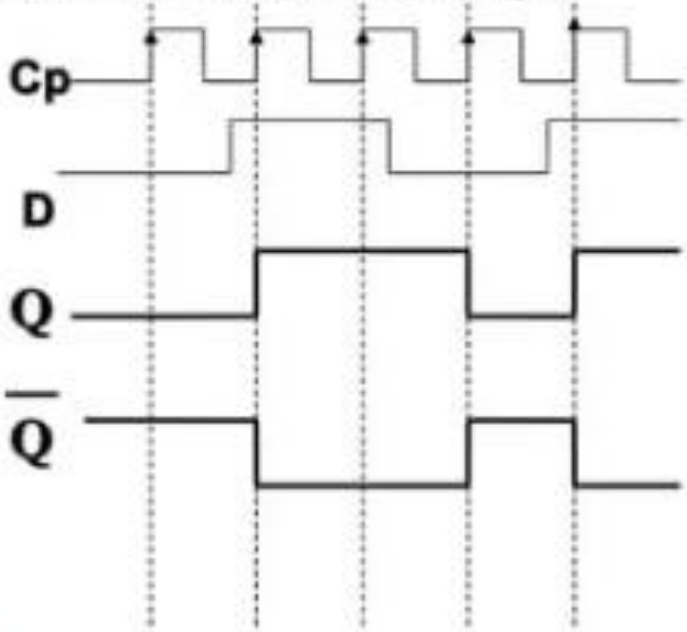


- **Figure 4.6.4:** Truth Table for D Flip Flop

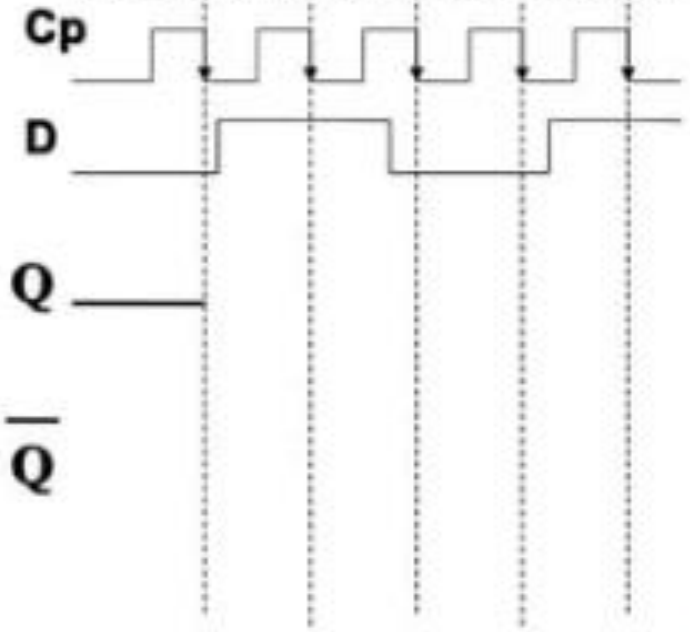
D	clock	Q	$\bar{Q}$	status
0	↑	0	1	RESET
1	↑	1	0	SET

4.6 D Flip Flop – Waveforms

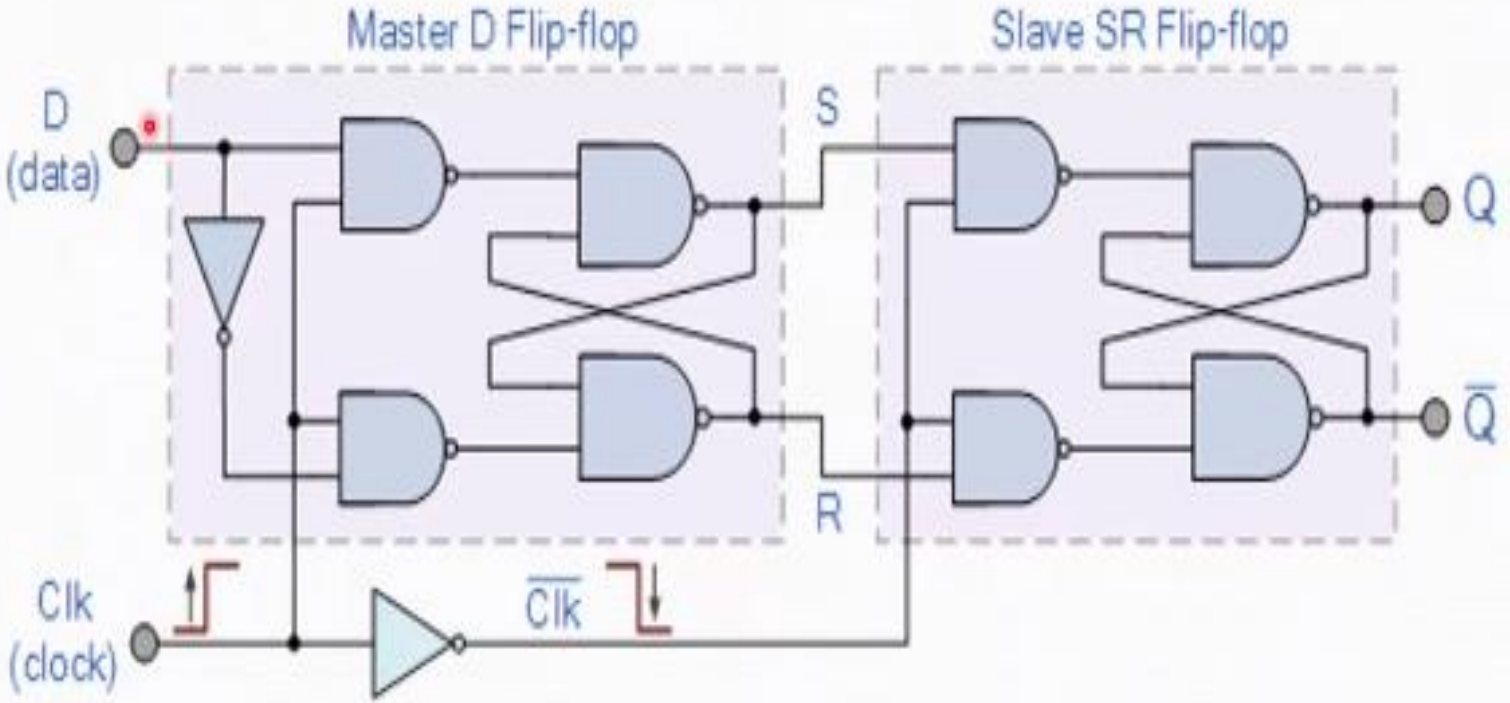
Example 4.6.1 : Determine the output of **PGT D** flip flop for the given input waveforms which the **Q initially 0.**



- **Exercise 4.6.1** Determine the output of **NGT D** flip flop for the given input waveforms, which output Q initially 0.



Master-Slave D flip-flop



3.2.1 RS Flipflop consisting of NOR Gates

❒ Experiment 1: Fundamental principles

Examine the RS flipflop in fig. 3.2.1.1.

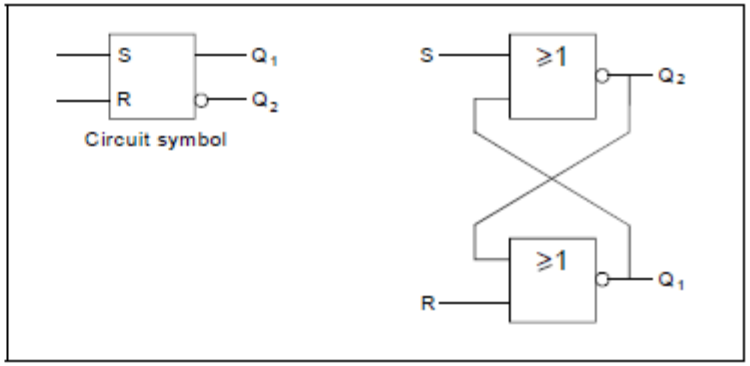


Fig. 3.2.1.1 Circuit

Experiment procedure:

- Set up the circuit shown in fig. 3.2.1.1.
- Apply the values specified in table 3.2.1.1 one after the other to the inputs S and R of the circuit and fill in the missing output values for Q_1 and Q_2.
- Explain the behaviour of the flipflop in table 3.2.1.1 with the terms **set, reset, store, not defined** (stored output state is random if S and R change from H to L at the same time) and **irregular** (Q_1 and Q_2 have no opposite levels).

S	R	Q_1	Q_2	Explanation
0	0	0	1	Store
1	0	1	0	Set
0	0	1	0	Store
0	1			
0	0			
1	1			
1 → 0	1 → 0	0	1	
		1	0	

3.2.2 RS Flipflop consisting of NAND Gates

❒ Experiment 1: Fundamental principles

Examine the RS flipflop in fig. 3.2.2.1.

Experiment procedure:

- Set up the circuit shown in fig. 3.2.2.1.
- Complete the table 3.2.2.1.

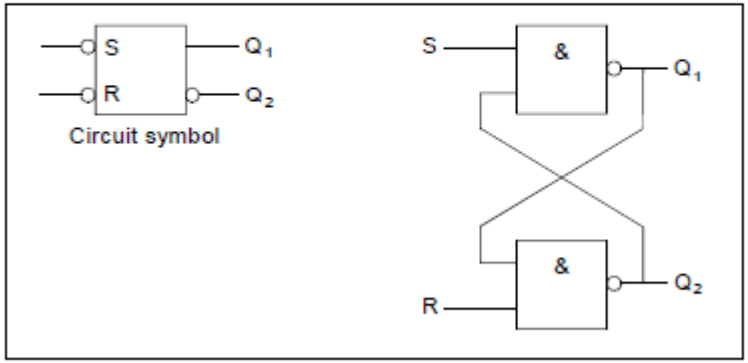


Fig. 3.2.2.1 Circuit

t_n		t_{n+1}		Explanation
S	R	Q_1	Q_2	
0	0			
0	1			
1	0			
1	1			
0 → 1	0 → 1			

Table 3.2.2.1

3.2.3 Clock State Controlled RS Flipflops

❒ Experiment 1: One state controlled RS flipflop

In many cases it is undesirable for the output state of the flipflop to change even only a few nanoseconds after the input state changes. Clock state controlled RS flip-flops were developed for this reason.

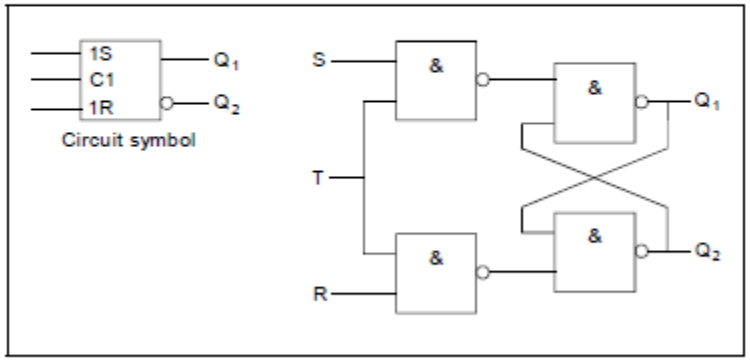


Fig. 3.2.3.1 Circuit

Experiment procedure:

- Set up the circuit as shown in fig. 3.2.3.1. The clock is treated here as a third binary input.

- Complete the table 3.2.3.1 and the pulse diagram in fig. 3.2.3.2.

N. B.:
The pulse diagram in fig. 3.2.3.2 shows the disadvantage of one state controlled clock inputs. After the clock, the state of the flipflop corresponds to the **last** information at the end of the clock. The probability of errors as a result of this can be kept low if a **small** enough clock duration is selected.

Clock T	S	R	Q_1	Q_2	Explanation
0	0	0			
0	1	0			
0	0	1			
0	1	1			
1	0	0			
1	1	0			
1	0	1			
1	1	1			

Table 3.2.3.1

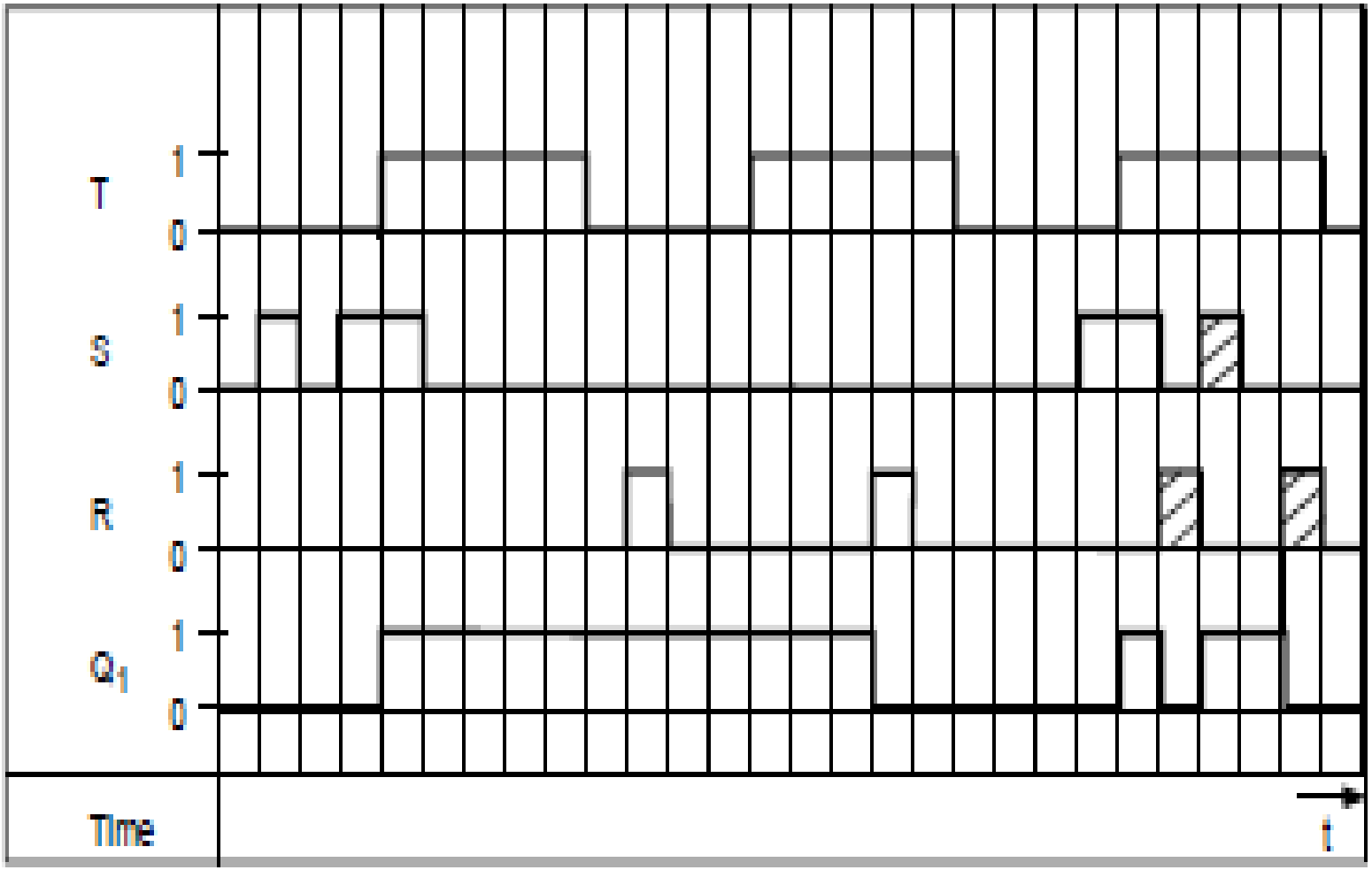


Fig. 3.2.3.2 Pulse diagram

3.2.5 D Flipflops

❒ Experiment 1: Fundamental principles

Flipflops with one state controlled clock inputs are often used as binary memory components. They are then usually designed as D flipflops.

Examine the D flipflop in fig. 3.2.5.1.

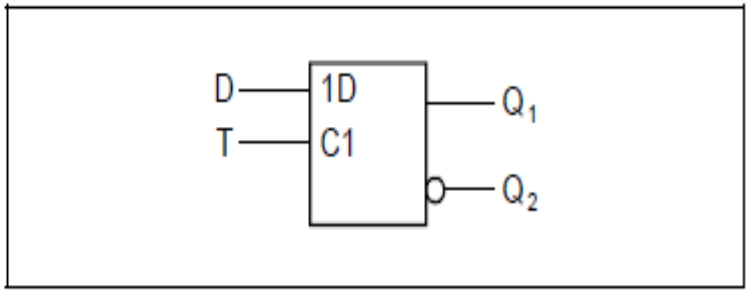


Fig. 3.2.5.1 Circuit symbol

Experiment procedure:

- Set up the circuit as shown in fig. 3.2.5.1.
- Examine the function by completing the value table (table 3.2.5.1).

Clock T	D	Q_1	Q_2
1	0		
1	1		

Table 3.2.5.1

❒ Experiment 2:

As far as its function is concerned, the D flipflop with state controlled clock input can be considered as a corresponding RS flipflop in which only permissible switching states exist.
Set up this circuit. Only NAND gates are available.

Experiment procedure:

- Complete the circuit in fig. 3.2.5.2 and then enter the levels for transferring a „0" or a "1" into the circuit.
- Check the circuit with the Digital Training System.

N. B.:
This flipflop only has permissible switching states because only a NAND element can have 0 state at the input. This guarantees that the state required for switching can only occur at either D4 or D5.

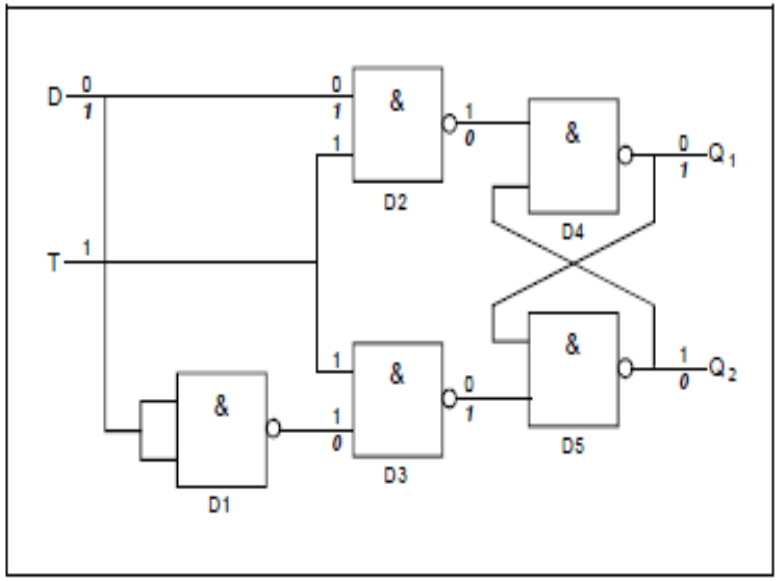


Fig. 3.2.5.2 Circuit

3.2.6 Single Edge Controlled RS Flipflop

❒ Experiment 1: Fundamental principles

The susceptibility to disturbance of the clock state controlled RS flipflop (see chapter 3.2.3, page 35) can be further reduced if setting or resetting of a flipflop is only possible during the edge of the clock pulse.

Technically the edge control can be realized with a CR circuit and a diode for inhibiting the negative or positive needle pulses (differentiator).

Fig. 3.2.6.1 shows the circuit symbol and fig. 3.2.6.2 the circuit for the principle of a singled edge controlled RS flipflop without using a differentiator.

Experiment procedure:

- Set up the circuit as shown in fig. 3.2.6.2.
- Check the function of the circuit with the Digital Training System and complete the pulse diagram in fig. 3.2.6.3.

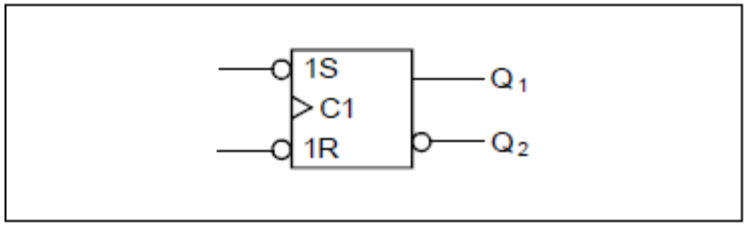


Fig. 3.2.6.1 Circuit symbol

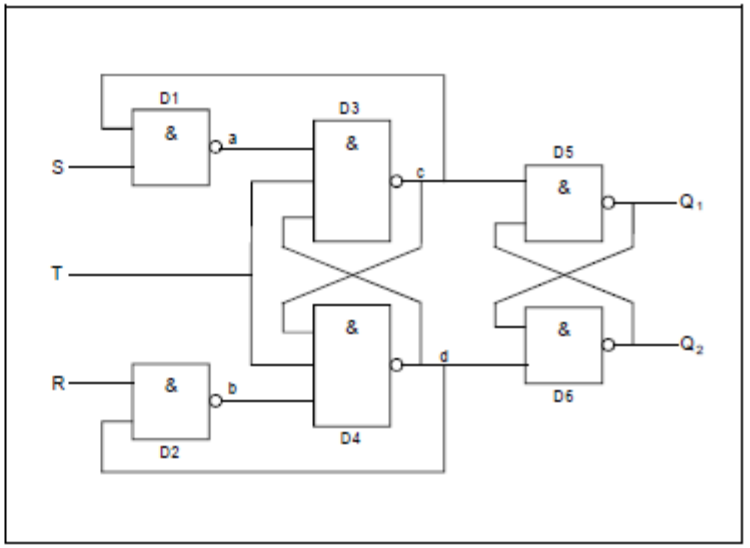
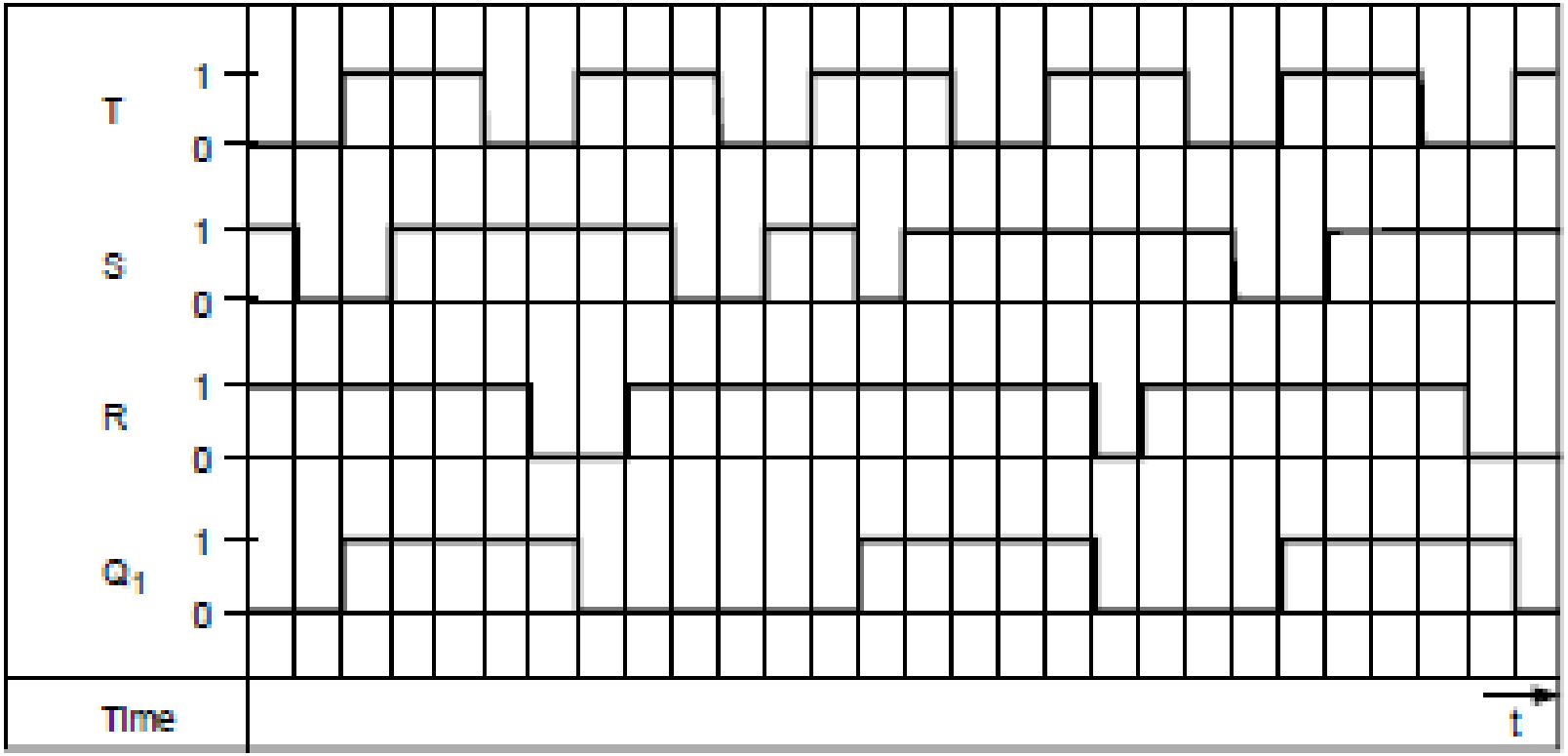


Fig. 3.2.6.2 Circuit

3.2.6 Single Edge Controlled RS Flipflop

❒ Experiment 1: Fundamental principles



3.2.7 Two State Controlled D Flipflop

❒ Experiment 1: Master-slave control

The D-flipflop is suitable as a basic element for read and write memories (RAM).
If a **simultaneous** evaluation of the output states (read) and new reading in (write) is to be enabled, the flipflop must be equipped with a master-slave control. The circuit symbol in fig. 3.2.7.1 and the reserve circuit diagram in fig. 3.2.7.2 should explain this. Use the inverter on the DIGI BOARD 2 and connect it to high level. If the circuit is in undefinated state you have to realize the original state according to Fig. 3.2.7.3.

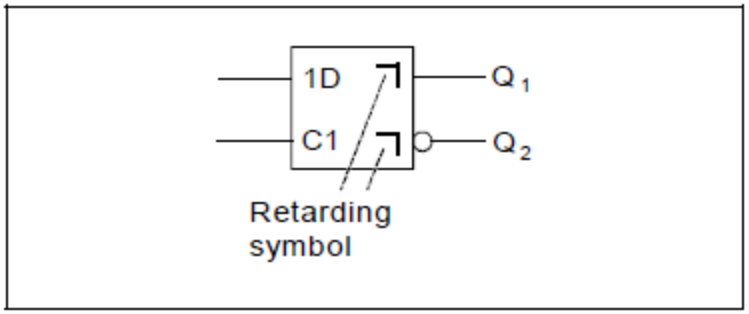


Fig. 3.2.7.1 Circuit symbol

Experiment procedure:

- Set up the circuit as shown in fig. 3.2.7.2 and test it th the Digital Training System.

- Complete the pulse diagram in fig. 3.2.7.3.

N. B.:
The two-state controlled D flipflop passes on the information at the **end of the clock pulse** from the data input to the output Q_1 **until the clock pause starts**.

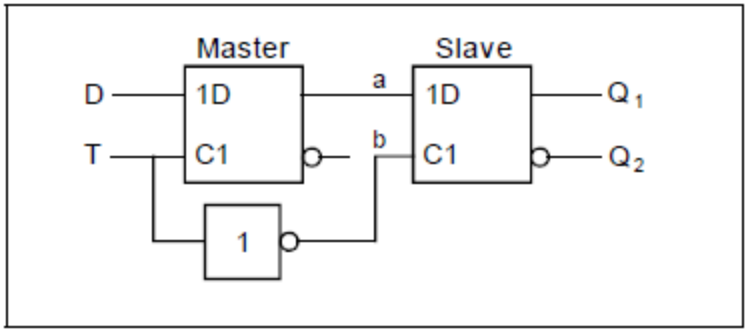


Fig. 3.2.7.2 Reserve circuit diagram

❒ Experiment 2: Dynamic J and K input

Experiment procedure:

- Determine the reserve flipflop for the wiring in fig. 3.2.8.3 by completing the table 3.2.8.2.

- Complete the reserve flipflop in fig. 3.2.8.4.

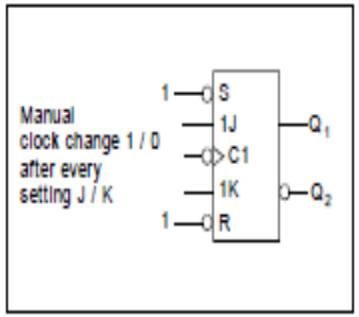


Fig. 3.2.8.3

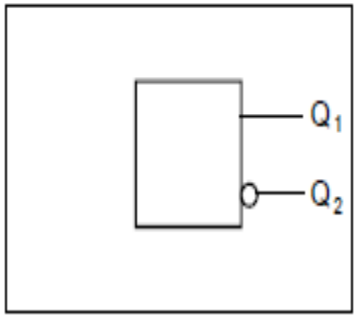


Fig. 3.2.8.4

Clock	J	K	Q_1	Q_2	Explanation
1 → 0	1	0			
1 → 0	0	0			
1 → 0	0	1			
1 → 0	1	1			
1 → 0	1	1			
1 → 0	1	0			
1 → 0	0	0			

Table 3.2.8.2 Value table