Arithmetic Circuits
Adders

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Arithmetic Circuits Definition

An arithmetic circuit is a set of gates with a separate set of inputs for each number that has to be processed. The gates are connected so as to carry out an arithmetic action and the outputs of the gate circuit are the digits of the result (addition, subtraction, multiplication, or division).

TYPES OF BINARY ADDER

- Half Adder(semi)
- Full Adder

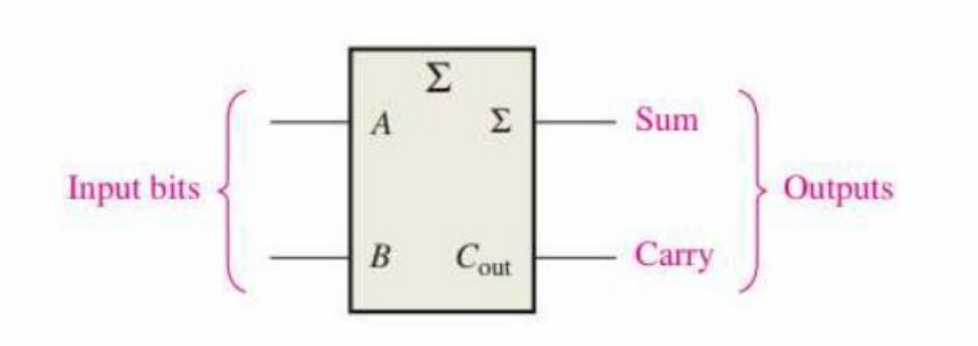
Half Adder

- Recall the basic rules for binary addition

$$
\begin{aligned}
0 + 0 &= 0 \\
0 + 1 &= 1 \\
1 + 0 &= 1 \\
1 + 1 &= 10
\end{aligned}
$$

- The operations are performed by a logic circuit called a half-adder

- The half-adder accepts two binary digits on its inputs and produces two binary digits on its outputs—a sum bit and a carry bit.



Logic symbol for a half-adder

TABLE 6–1

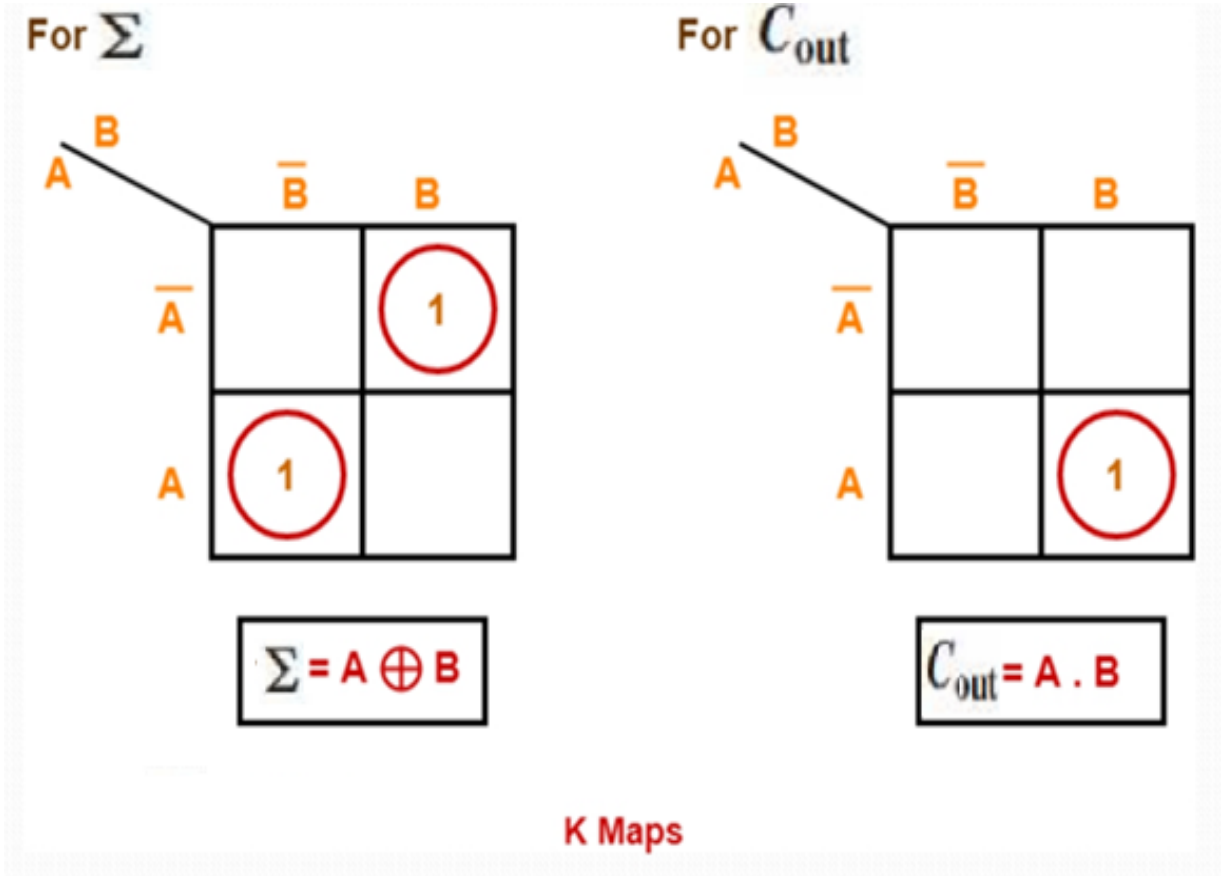
Half-adder truth table.

A	B	C_{out}	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Σ = sum

C_{out} = output carry

A and B = input variables (operands)



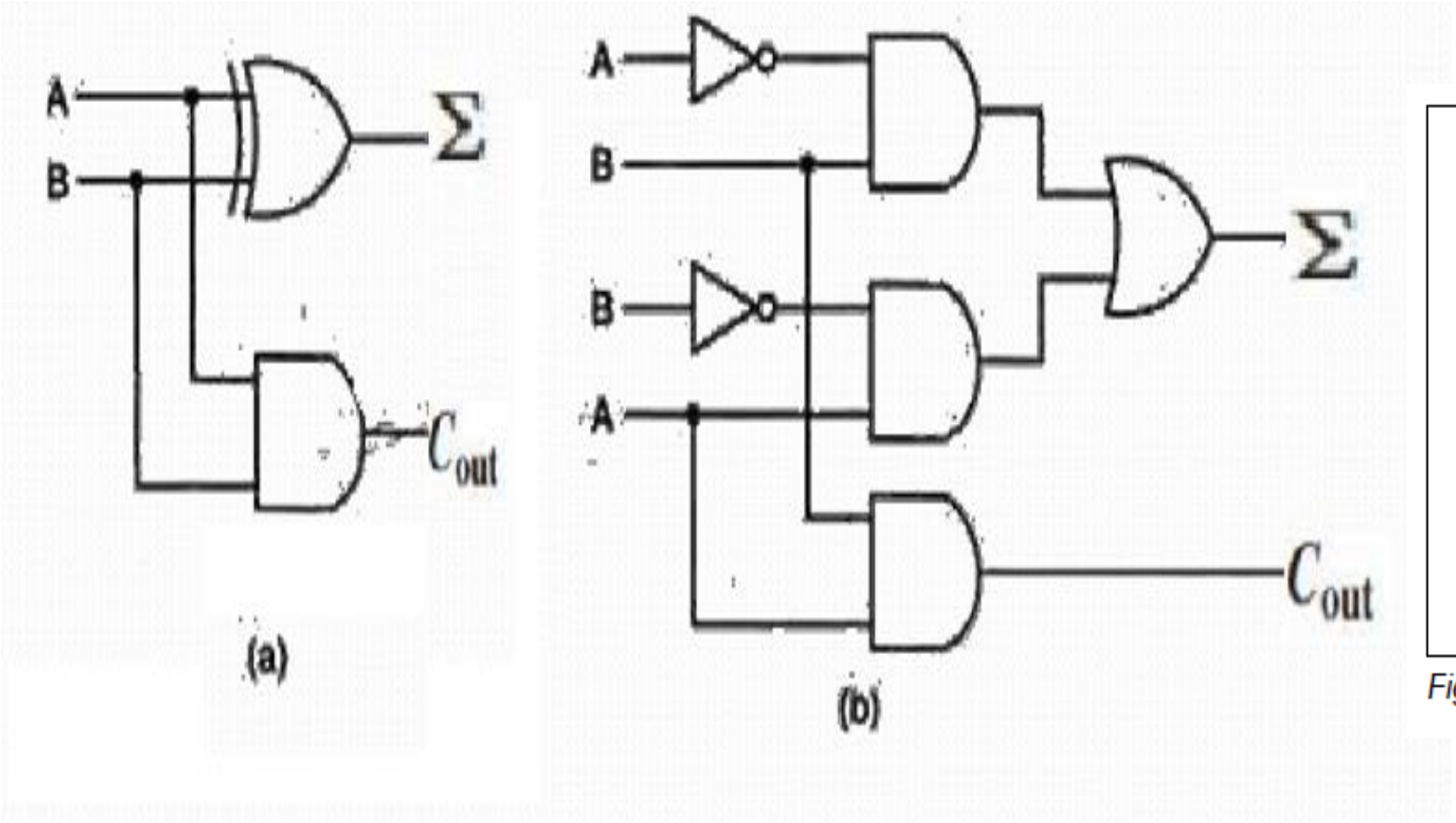
- Now observe that the sum output is a 1 only if the input variables, A and B, are not equal. The sum can therefore be expressed as the exclusive-OR of the input variables.

$$\Sigma = A \oplus B$$

- Notice that the output carry is a 1 only when both A and B are 1s;therefore, Cout can be expressed as the AND of the input variables.

$$C_{out} = AB$$

Logic Diagram



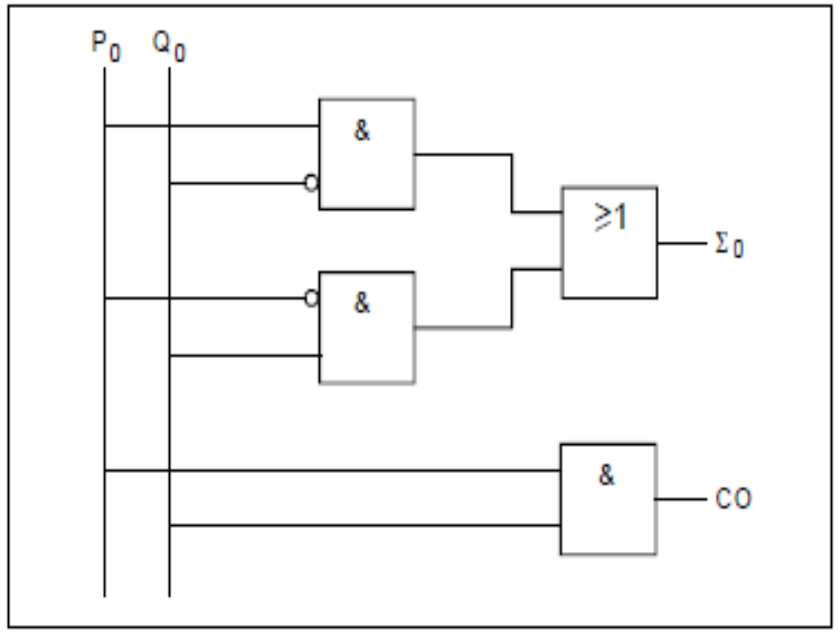
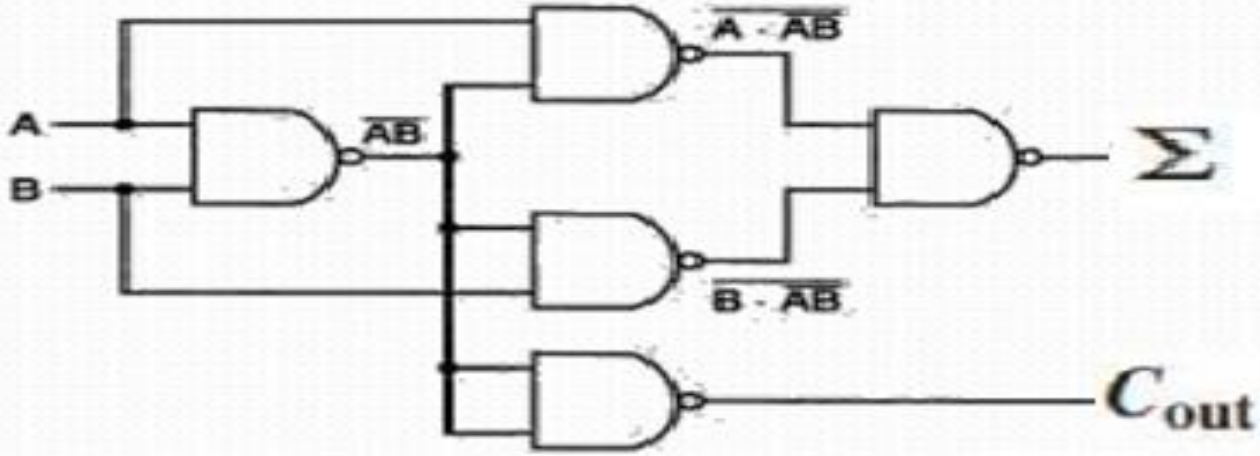


Fig. 6.1.2.2 Circuit of a semi adder

HALF ADDER (Using only NAND Gate)

$$\Sigma = A\bar{B} + \bar{A}B = A\bar{B} + A\bar{A} + \bar{A}B + B\bar{B}$$
$$= A(\bar{A} + \bar{B}) + B(\bar{A} + \bar{B})$$
$$= A \cdot \overline{AB} + B \cdot \overline{AB}$$
$$= \overline{A \cdot \overline{AB} \cdot B \cdot \overline{AB}}$$
$$C_{out} = AB = \overline{\overline{AB}}$$

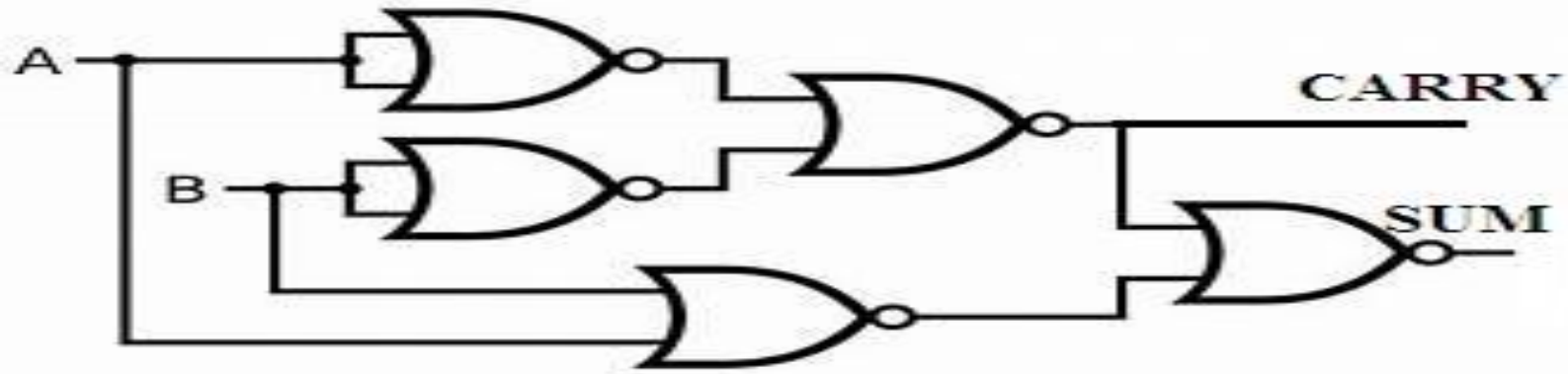


Logic diagram of a half-adder using only NAND gates.

HALF ADDER (Using NOR Gate)

$$\Sigma = A\bar{B} + \bar{A}B = A\bar{B} + A\bar{A} + \bar{A}B + B\bar{B}$$
$$= A(\bar{A} + \bar{B}) + B(\bar{A} + \bar{B})$$
$$= (A + B)(\bar{A} + \bar{B})$$
$$= \overline{\overline{A + B} + \overline{\bar{A} + \bar{B}}}$$

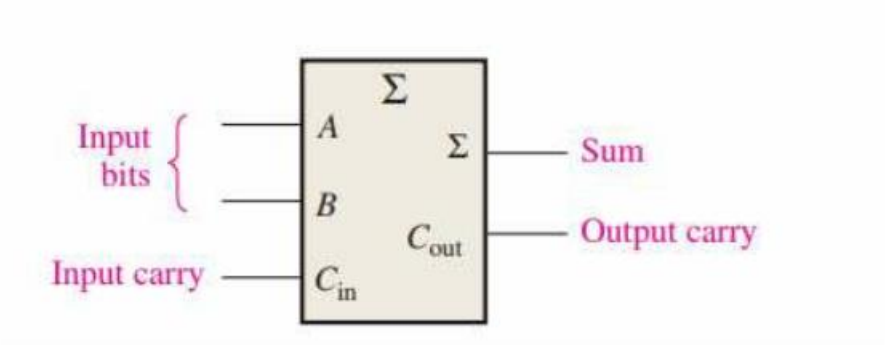
$$C_{out} = AB = \overline{\overline{AB}} = \overline{\bar{A} + \bar{B}}$$



Logic diagram of a half-adder using only NOR gates.

Full Adder

- The full-adder accepts two input bits and an input carry and generates a sum output and an output carry.
- The basic difference between a full-adder and a half-adder is that the full-adder accepts an input carry



Logic symbol for a full-adder.

TABLE 6–2

Full-adder truth table.

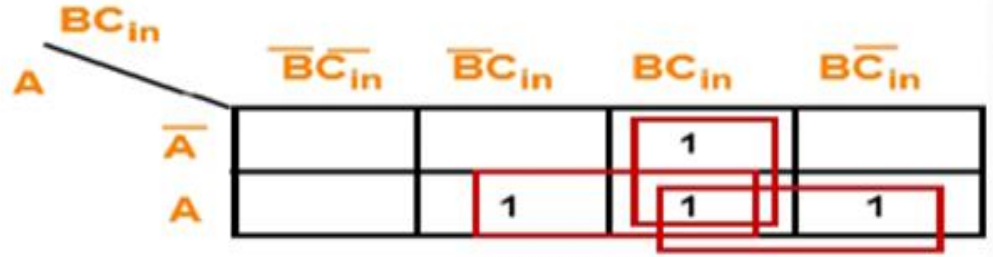
A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

C_{in} = input carry, sometimes designated as *CI*
C_{out} = output carry, sometimes designated as *CO*
Σ = sum
A and B = input variables (operands)

For $\sum$

$$\Sigma = (A \oplus B) \oplus C_{in}$$

For C_{out}



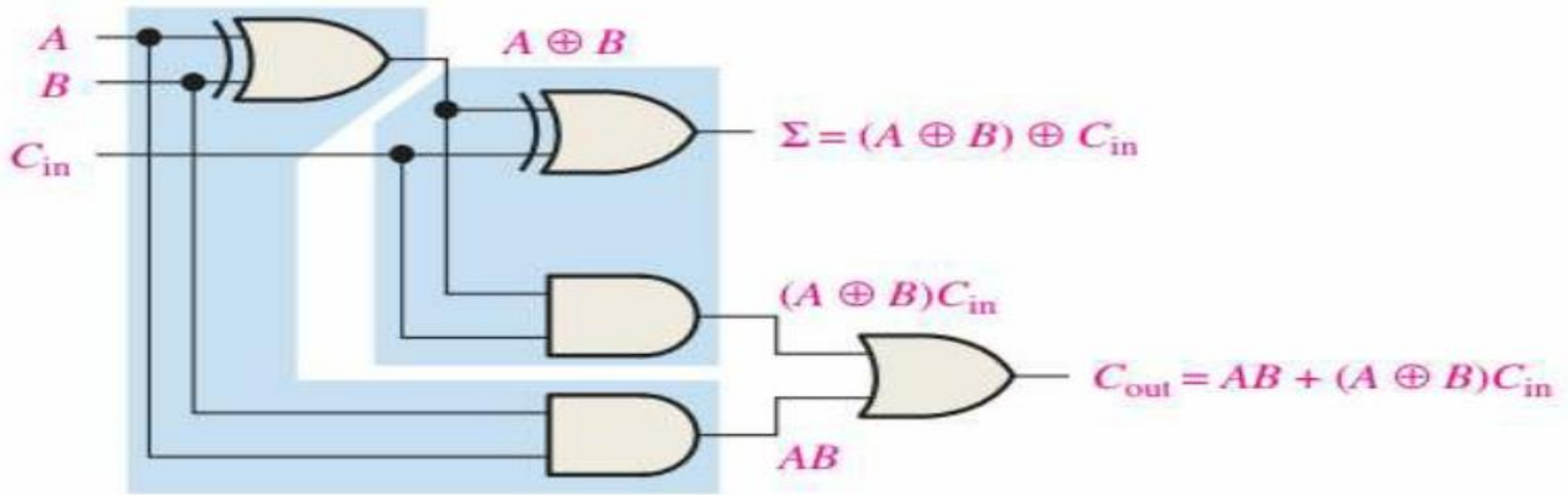
$C_{out} = AB + BC_{in} + C_{in}A$

$\sum = \bar{A}\bar{B}Cin + ABCin + \bar{A}B\bar{C}in + A\bar{B}\bar{C}in = Cin(A \odot B) + \bar{C}in(A \oplus B) = (A \oplus B) \oplus Cin$

Using SOP to find Co

$Co = \bar{A}BCin + A\bar{B}Cin + AB\bar{C}in + ABCin = Cin(\bar{A}B + A\bar{B}) + AB(\bar{C}in + Cin) = AB + Cin(A \oplus B)$

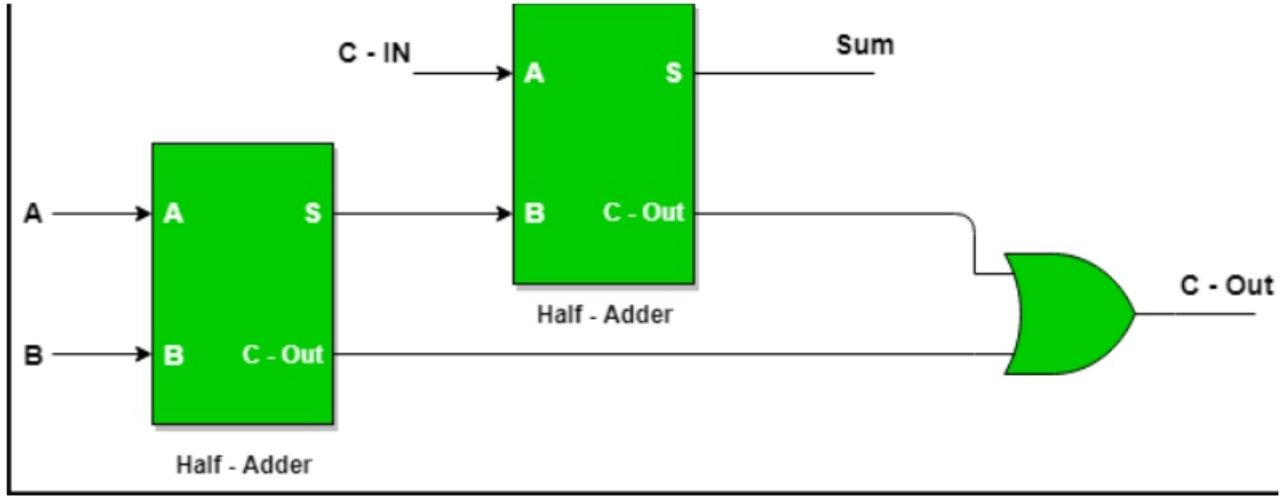
Logic circuit



(b) Complete logic circuit for a full-adder (each half-adder is enclosed by a shaded area)

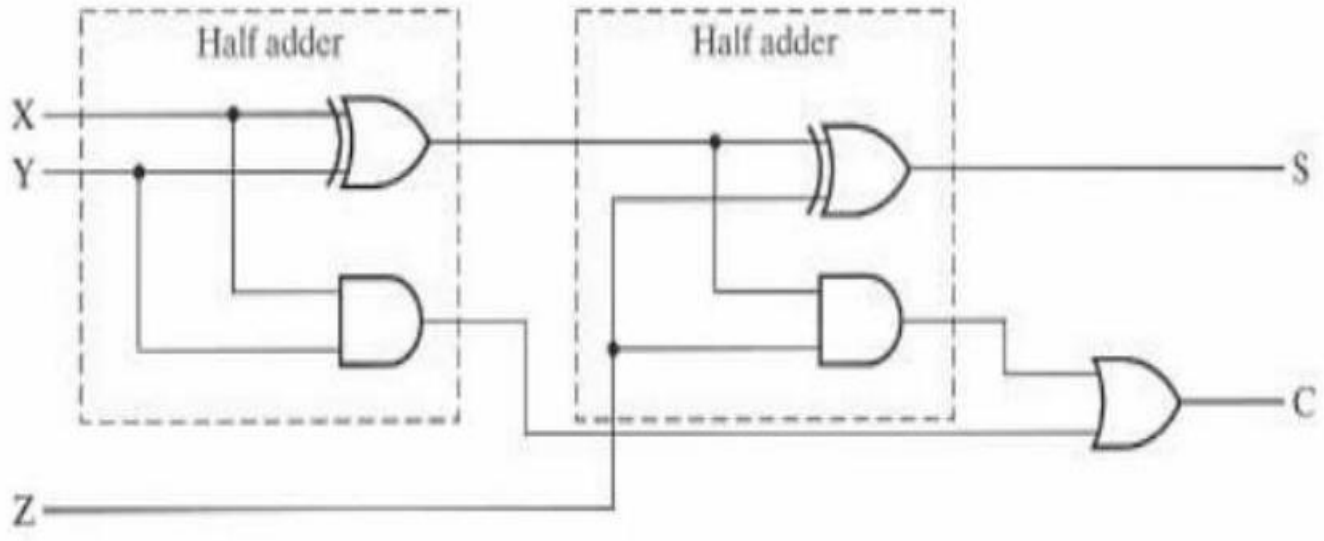
Implementation of Full Adder using Half Adders

- Two Half Adders and a OR gate is required to implement a Full Adder.



Block diagram of full adder using two half adder

Implementation of Full Adder using Half Adders

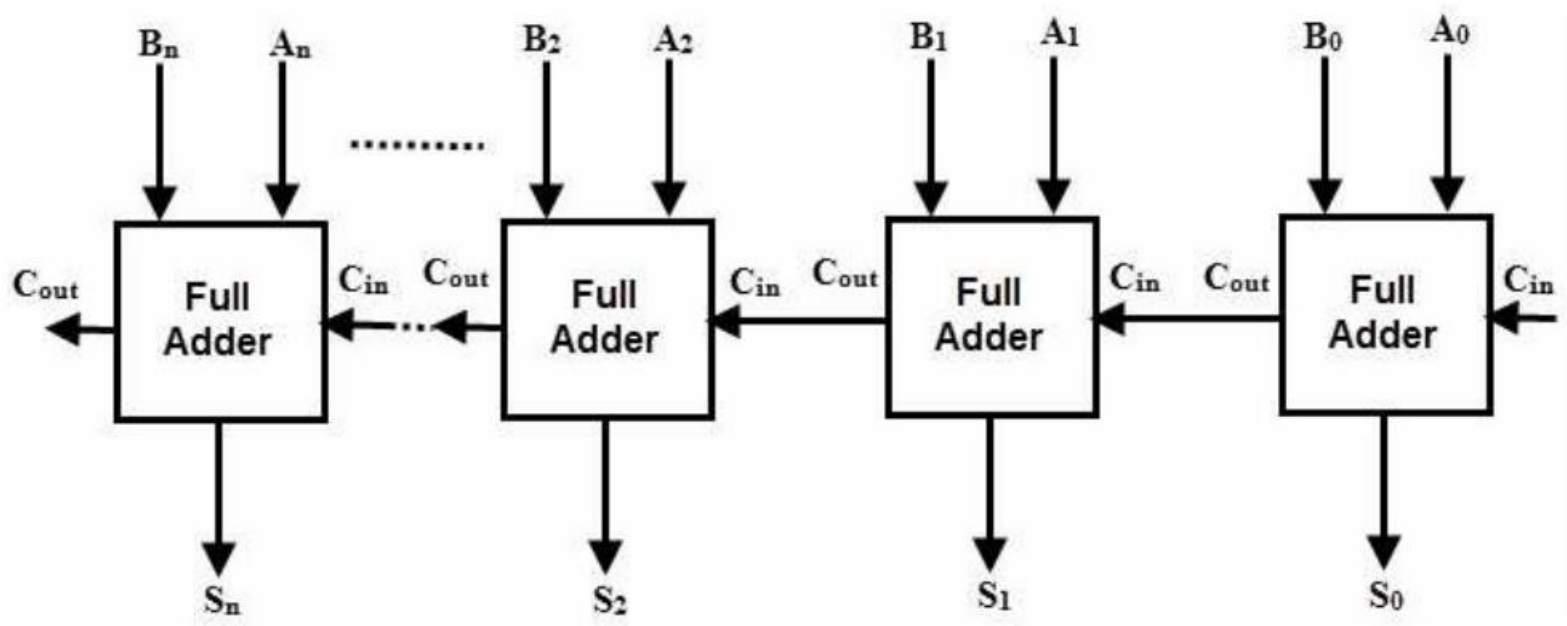


Logic circuit of full adder using two half adder

Parallel Binary Adders

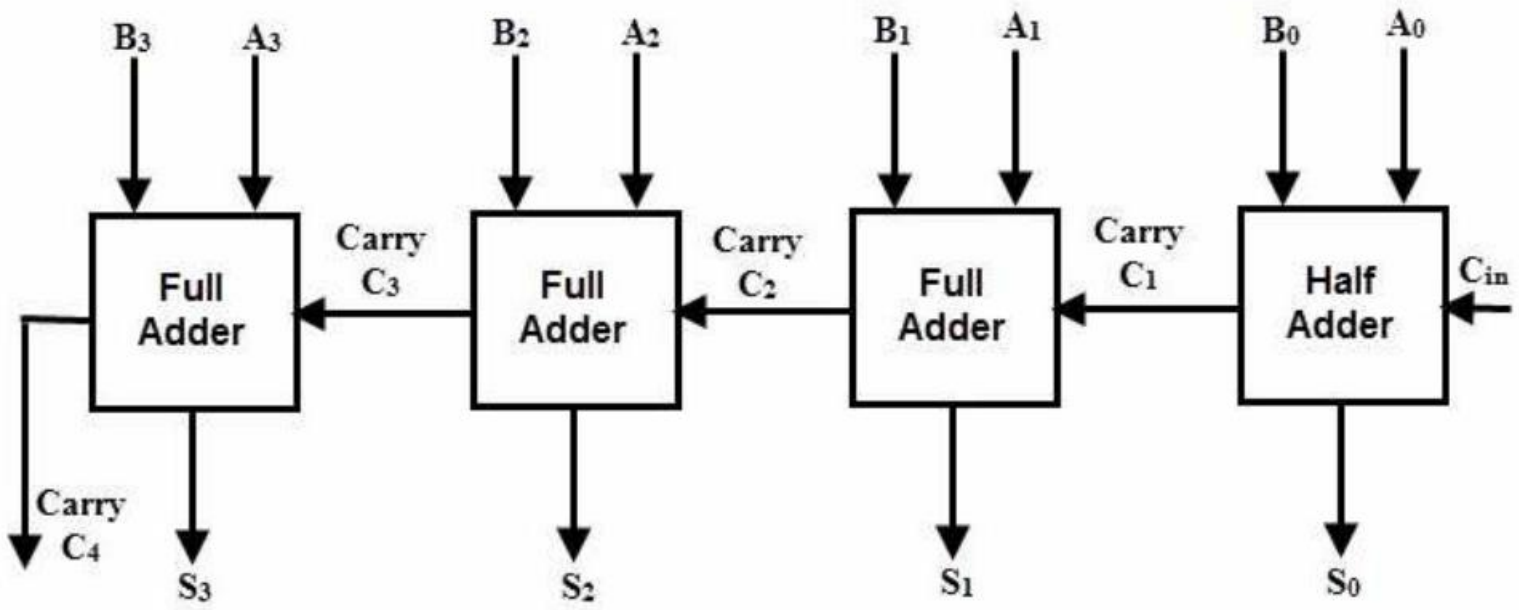
- As we discussed that a single full adder performs the addition of two one bit numbers and an input carry.
- For performing the addition of binary numbers with more than one bit, more than one full adder is required depends on the number bits.
- Thus, a parallel adder is used for adding all bits of the two numbers simultaneously.
- By connecting a number of full adders in parallel, n-bit parallel adder is constructed.

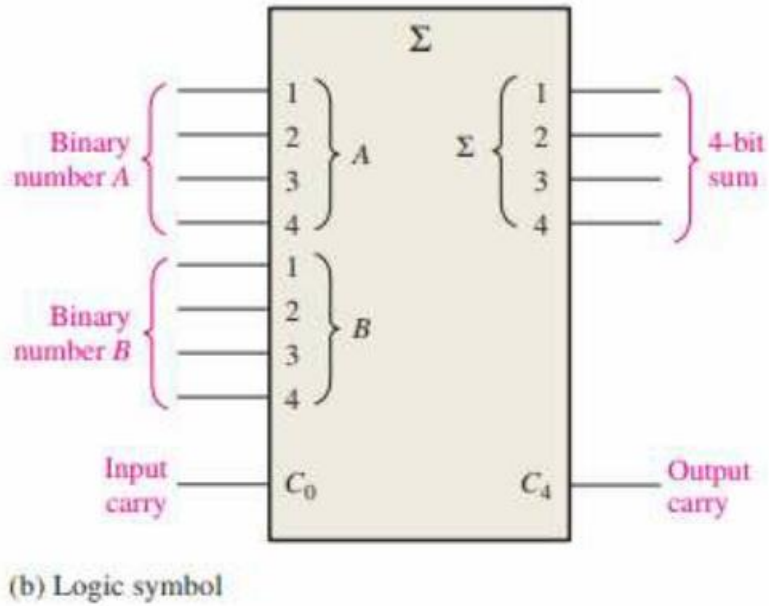
- It is to be noted that there is no carry at the least significant position, hence we can use either a half adder or made the carry input of full adder to zero at this position.



Four-Bit Parallel Adders

- A group of four bits is called a nibble.
- A basic 4-bit parallel adder is implemented with four full-adder.





(b) Logic symbol

- The two binary numbers to be added are A3A2A1A0 and B3B2B1B0 which are applied to the corresponding inputs of full adders.
- This parallel adder produces their sum as C4S3S2S1S0 where C4 is the final carry.
- In the 4 bit adder, first block is a half-adder(Or, Full adder) that has two inputs as A0B0 and produces their sum S0 and a carry bit C1. Next block should be full adder as there are three inputs applied to it. Hence this full adder produces their sum S1 and a carry C2. This will be followed by other two full adders and thus the final sum is C4S3S2S1S0.

- Most commonly Full adders are designed in dual in-line package integrated circuits.
- A typical 74LS283 is a 4 bit full adder.
- Arithmetic and Logic Unit of a unit computer consist of these parallel adders to perform the addition of binary numbers.

Adder Expansion

- The 4-bit parallel adder can be expanded to handle the addition of two 8-bit numbers by using two 4-bit adders

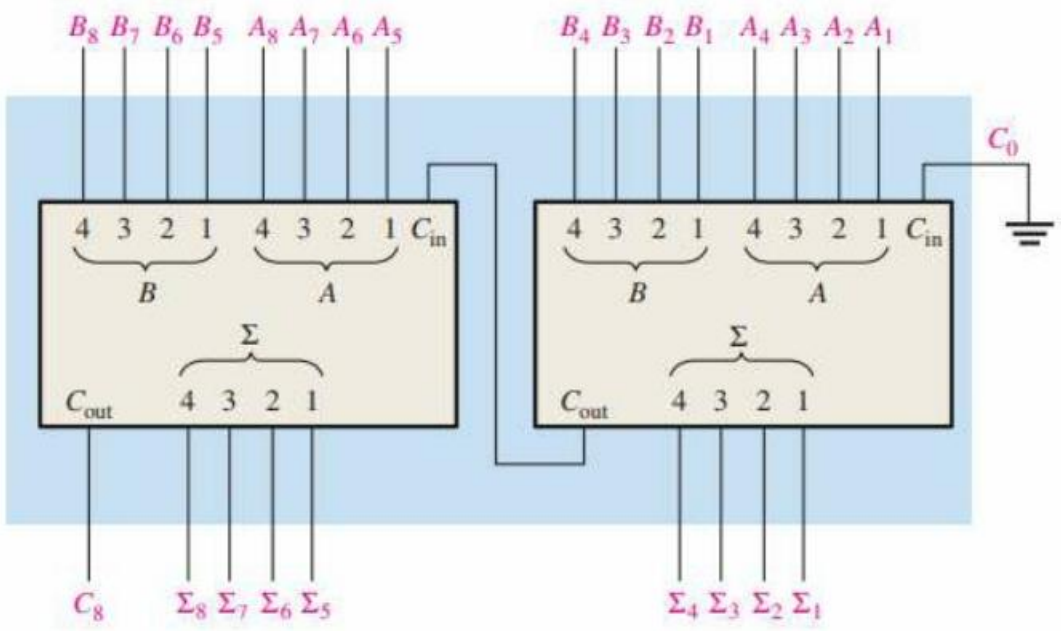


FIGURE 6–11 Cascading of two 4-bit adders to form an 8-bit adder.

6.2.1 Semi Adder

❒ Experiment 1: Semi adder consisting of basic elements

Experiment procedure:

- Design a semi adder consisting exclusively of basic elements and complete the circuit diagram for the adding circuit in fig. 6.2.1.1.
- Enter the output values of all gates for the specified input values in table 6.2.1.1.
- Check that the circuit and table are correct with the Digital Training System.

Summands		Gate outputs				Sum	
P_0	Q_0	D1	D2	D3	D4	Σ_0	C_1
0	0						
0	1						
1	0						
1	1						

Table 6.2.1.1

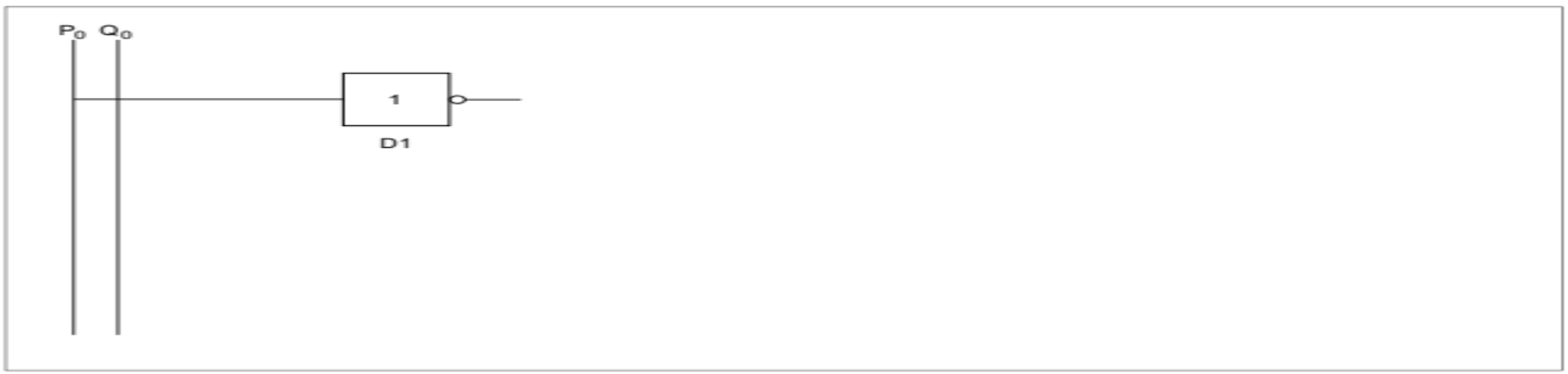


Fig. 6.2.1.1 Circuit for a semi adder consisting of basic elements

❒ Experiment 2: Semi adder consisting exclusively of NAND elements

Experiment procedure:

- Design a semi adder consisting exclusively of NAND elements. Complete the circuit diagram for the adding circuit in fig. 6.2.1.2.
- Enter the output values of all gates for the specified input values in table 6.2.1.2.
- Check that the circuit and table are correct with the Digital Training System.
- The semi adder can also be set up with just two gates. Complete the circuit in fig. 6.2.1.3 and check it with the Digital Training System.

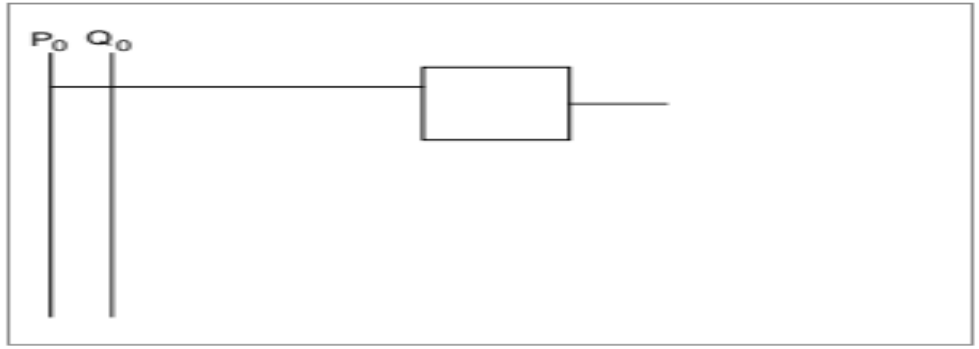


Fig. 6.2.1.3 Circuit

Summands		Gate outputs					Sum	
P_0	Q_0	D1	D2	D3	D4	D5	Σ_0	C_1
0	0							
0	1							
1	0							
1	1							

Table 6.2.1.2

Fig. 6.2.1.2 Circuit for a semi adder consisting exclusively of NAND elements

6.2.2 Full Adder

❒ Experiment 1 : 1-bit full adder

A 1-bit full adder should be set up with AND, OR and NOT elements.

Experiment procedure:

- Complete the table 6.2.2.1.
- Compose the minimized formulae for the sum Σ and the carry CO with the help of KV diagrams (fig. 6.2.2.1 and 6.2.2.2).
- Complete the circuit in fig. 6.2.2.3 and check the function with the Digital Training System.

P_1	Q_1	CI	Σ	CO
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
0	1	0		
1	1	1		

Table 6.2.2.1

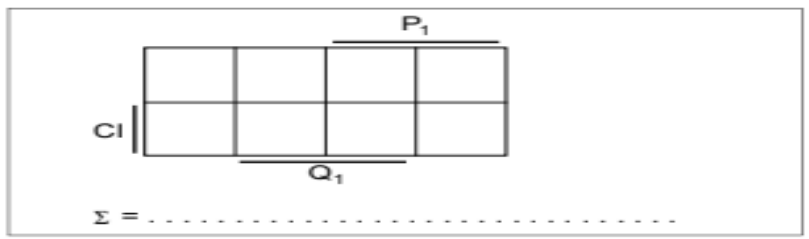


Fig. 6.2.2.1 KV diagram for Σ

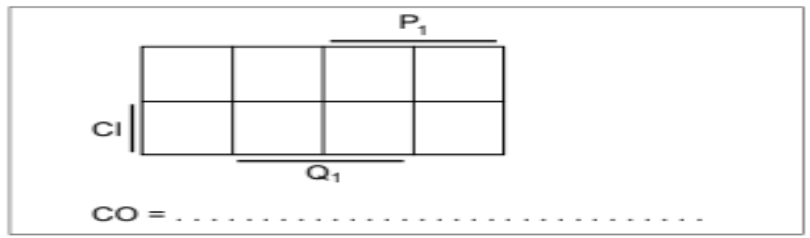


Fig. 6.2.2.2 KV diagram for CO

Fig. 6.2.2.3 Circuit for a 1-bit full adder

❒ Experiment 2: 2-bit full adder

A 2-bit full adder should be designed from discrete semi adders.

Experiment procedure:

- Complete table 6.2.2.2.
- Complete the circuit in fig. 6.2.2.4.
- Test the 2-bit full adder with the Digital Training System.
- Enter the values for addition of the dual numbers P = 01 and Q = 11 in the circuit diagram for checking.

P_1	Q_1	P_0	Q_0	CO	Σ_1	Σ_0
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

Table 6.2.2.2

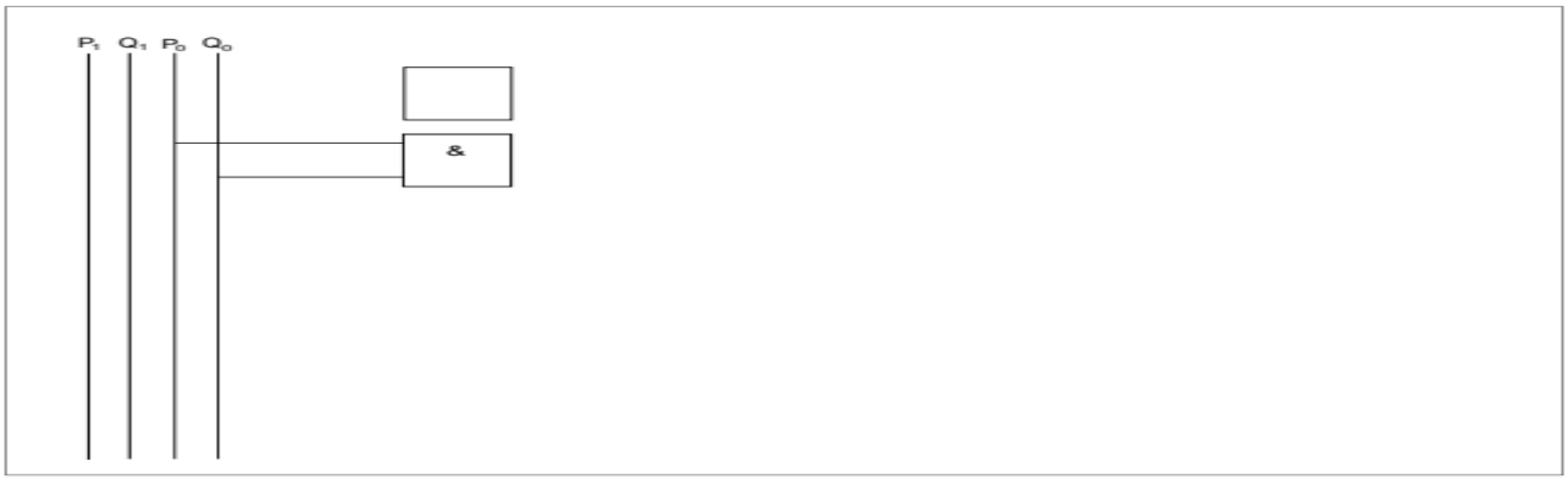


Fig. 6.2.2.4 Circuit for a 2-bit full adder