Arithmetic Circuits

Subtractor

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BINARY SUBTRACTOR

RULES FOR BINARY SUBTRACTION

0 - 0 = 0

0 - 1 = 1 with borrow 1

1 - 0 =1

1 – 1=0

NOTE: In the second case (0 – 1) it is necessary to borrow a 1.

TYPES OF BINARY SUBTRACTOR

- Half Subtractor
- Full Subtractor

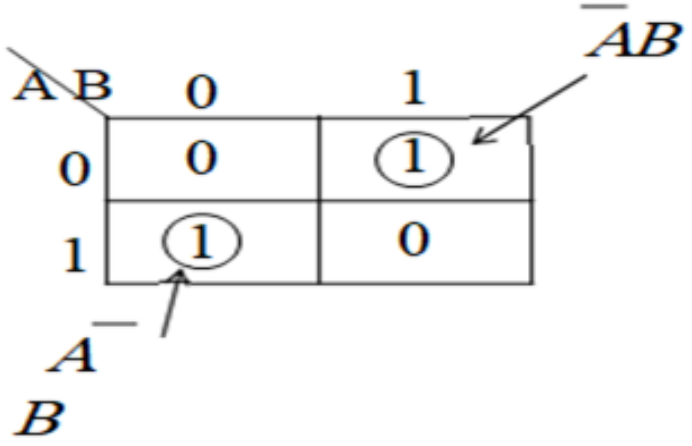
Half Subtractor:

- It is a combinational circuit with two inputs and two outputs (difference and borrow)
- Two inputs are X (minuend), Y (subtrahend) and two outputs are D (difference) and B (borrow out).
- It is used to perform subtraction of two bits.

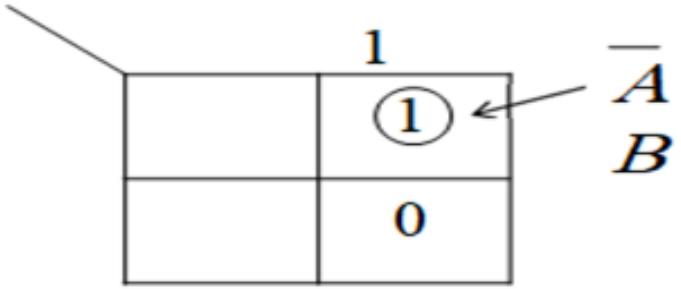
Half subtractor truth table :

INPUTS		OUTPUTS	
Minuend (A)	Subtrahend (B)	Difference (D)	Borrow (B_o)
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

K-Map for difference (D)



K-Map for Borrow Output (B_o)

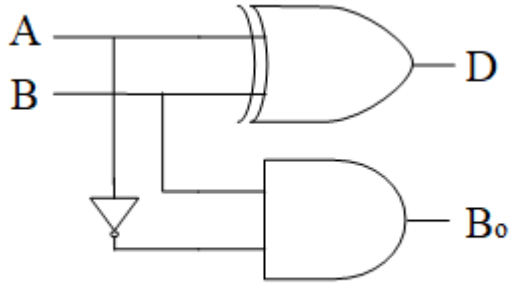


From K-maps

$$D = \overline{A}B + A\overline{B}$$

$$B = \overline{A}B$$

Half subtractor circuit diagram



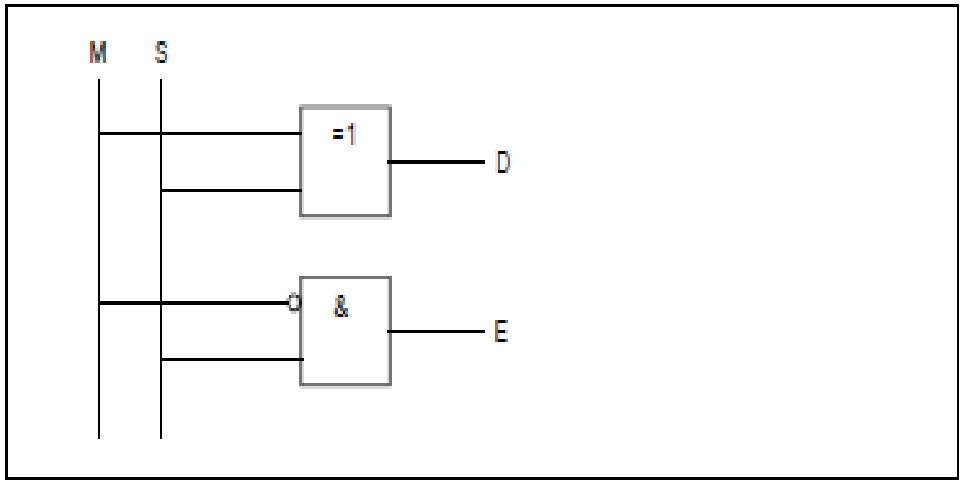
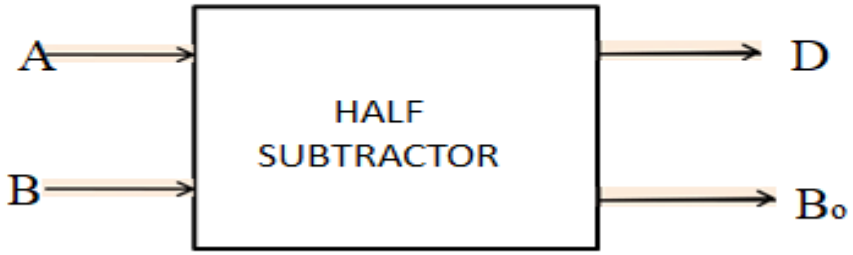


Fig. 6.2.4.2 Circuit 2

BLOCK DIAGRAM:

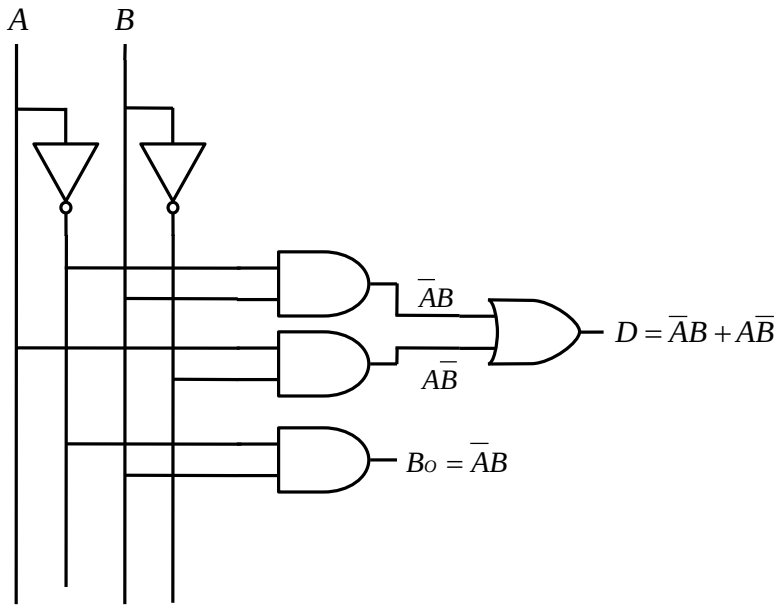


DISADVANTAGE OF HALF SUBTRACTOR:

Half subtractor can only perform the subtraction of two binary bits. But

while performing the subtraction, it does not take into account the borrow of the lower significant stage.

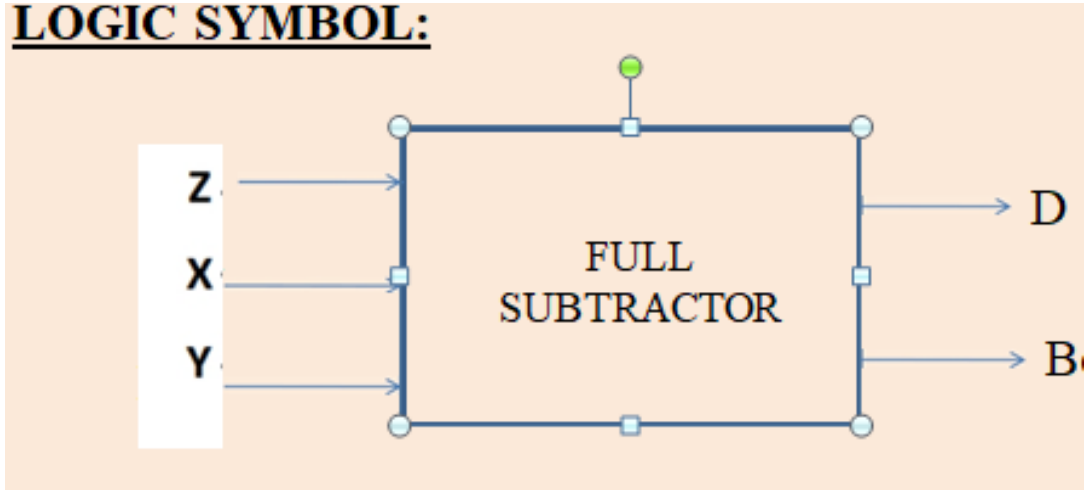
HALF SUBTRACTOR USING BASIC GATES:



Full Subtractor

- When there is a situation where the minuend and subtrahend number contains more significant bit, then the **borrow** bit which is obtained from the subtraction of 2-bit binary digits is subtracted from the next higher order pair of bits. In such situation, the subtraction involves the operation of 3 bits. Such situation of subtraction can't handle by a simple half subtractor. So, combining two half subtractor we can form another combinational circuit which can perform this type of operation. This circuit is known as the full subtractor.

- So we can define full subtractor as a combinational circuit which takes three inputs and produces two outputs **difference** and **borrow**. Below is the truth table of the full subtractor, we have used three input variables X, Y and Z which refers to the term **minuend, subtrahend** and **borrow** bit respectively.
  The two outputs **difference** and **borrow** are named as D and B respectively.



Full subtractor truth table

Inputs			Outputs	
M	S	E_1	D	E_2
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

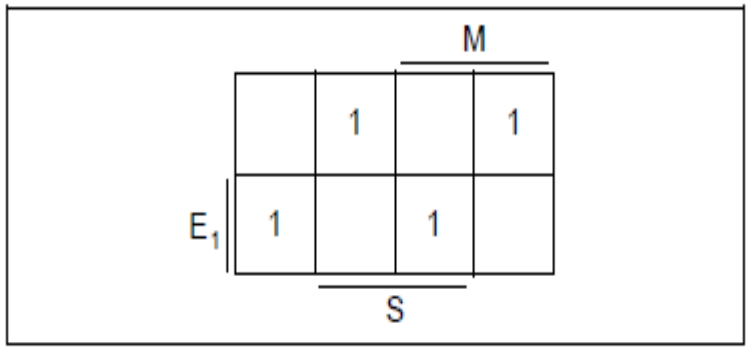


Fig. 6.2.5.1 KV diagram for D

$$D = \overline{M}\,\overline{S}\,E_1 \vee \overline{M}\,S\,\overline{E}_1 \vee M\,\overline{S}\,\overline{E}_1 \vee M\,S\,E_1$$

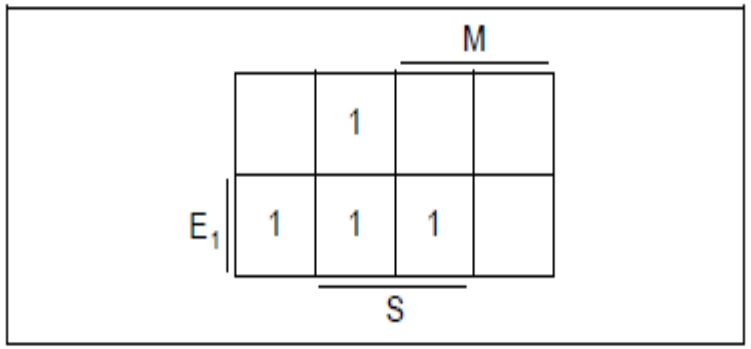
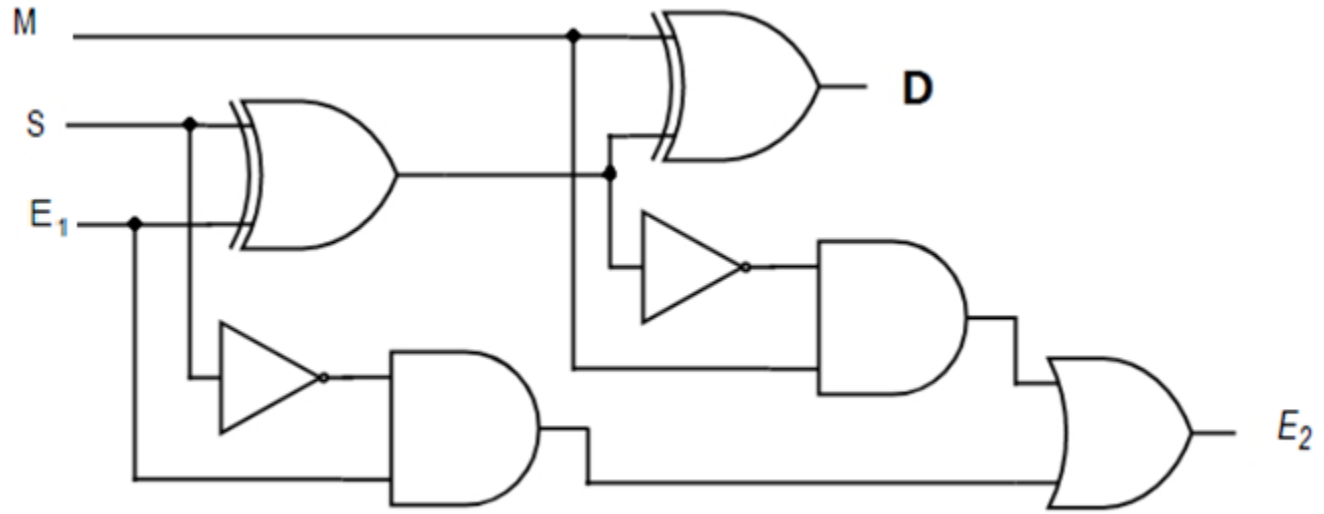


Fig. 6.2.5.2 KV diagram for E_2

$$E_2 = \overline{M}\,E_1 \vee \overline{M}\,S \vee E_1\,S$$

Full subtractorcircuit diagram



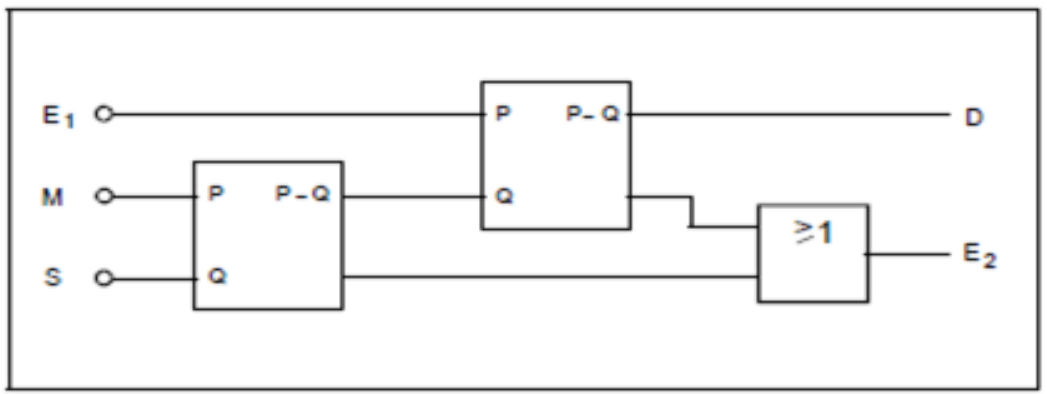
• Equation for a borrow output is resembles the carry output of full adder except that one of the input is complemented.

• Equation for D is same as the sum of output for a full adder.

design 1 bit full subtractor by using two half subtractor

$D = M - S - E_1$

The difference of M - S is formed by the first semi subtractor and the resulting sub-difference forms the result of the subtraction with E_1.

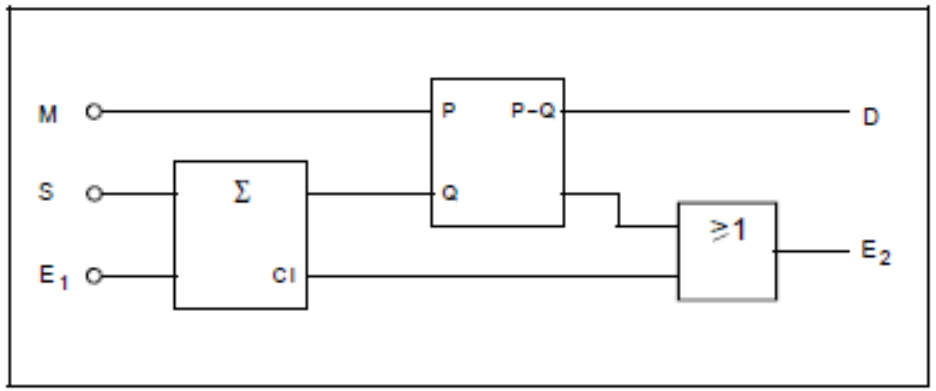


design 1 bit full subtractor by using half adder and half subtractor

Difference = minuend - (subtrahend + borrow)

$D = M - (S + E_1)$

The sum of S + E_1 is formed by a **semi adder**, the resultant **subtotal** then allow-s the **difference** to be formed with a **semi subtractor**.



6.1.5 Subtractor for Dual Numbers

In arithmetic units the subtraction is converted into an addition by adding the complement of the subtrahend Q to the minuend P.

```
   7      minuend P
-  5      subtrahend Q
+  2      result Σ with sign „+“

P     0 1 1 1
Q     0 1 0 1
```

The 2s complement of Q is formed by inverting every bit (1s complement) and then adding a „1".

```
Q̄     1 0 1 0
    +         1
      1 0 1 1      2s complement of Q

    0 1 1 1        P
    + 1 0 1 1      2s complement
   -4 0 0 1 0
```

The carry produced in the complement addition is not part of the subtraction result but can be used for sign evaluation.
Since a positive sign is represented by a „0" in binary coded numbers, the carry must be negated in the circuit.

Fig. 6.1.5.1 shows the subtracting circuit when the minuend is greater than the subtrahend.

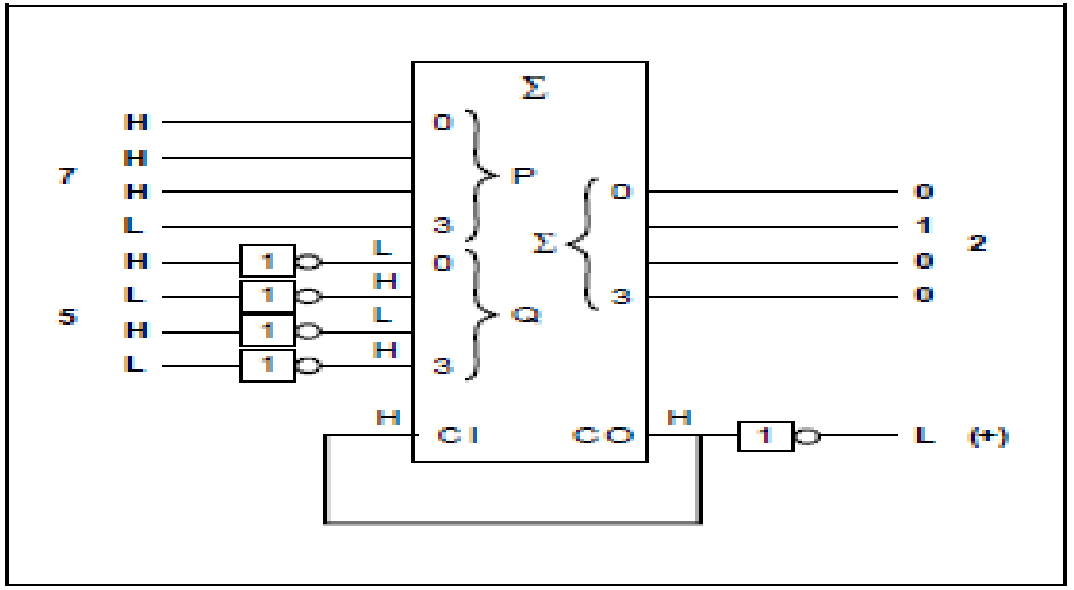


Fig. 6.1.5.1 Minuend > subtrahend

The 2s complement is formed by interconnection of CI and CO.

If the result of a subtraction is negative, 2s complement formation must also take place at the output:

```
   5      minuend P
 - 7      subtrahend Q
 - 2      result Σ with sign „-"

P     0 1 0 1
Q     0 1 1 1

Q̄     1 0 0 0
    +       1
      1 0 0 1     2s complement of Q

      0 1 0 1     P
    + 1 0 0 1     2s complement
    ⊖1 1 1 0      2s complement of
                  result Σ

      0 0 0 1     Σ̄
    +       1
      0 0 1 0
```

Fig. 6.1.5.2 shows the subtraction circuit when the minuend is smaller than the subtrahend.

In the circuit in fig. 6.1.5.2, addition of the „1" is omitted because it would have to be done at the input and the output.

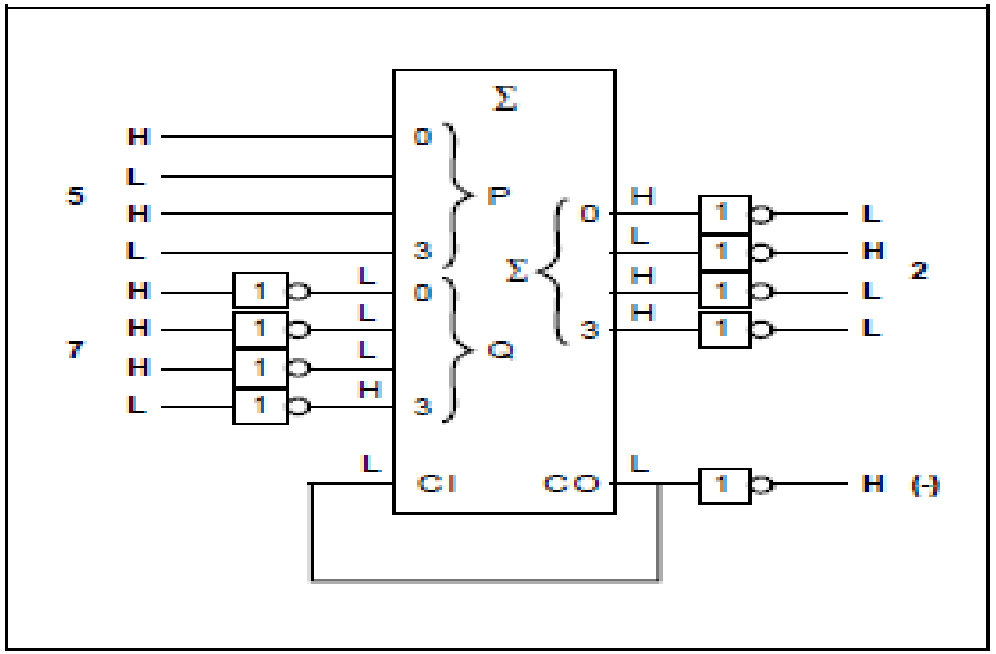


Fig. 6.1.5.2 Minuend < subtrahend

P - Q	CI	P_3	P_2	P_1	P_0	Q_3	Q_2	Q_1	Q_0	Σ_3	Σ_2	Σ_1	Σ_0	CO
7 - 5	1	0	1	1	1	0	1	0	1	0	0	1	0	1
5 - 3	1	0	1	0	1	0	0	1	1	0	0	1	0	1
7 - 4	1	0	1	1	1	0	1	0	0	0	0	1	1	1
9 - 9	1	1	0	0	1	1	0	0	1	0	0	0	0	1

Table 6.2.6.1