Counter

Eng. : Eman Abu Hani

Introduction to Counter

- The filp-flops are essential component in clocked sequential circuits.
- Circuits that include filp-flops are usually classified by the function they perform. Two such circuits are registers and counters.
- As the name suggests, it counts. The main purpose of counter is to count the number of occurrence of input .
- Counter is frequently used in digital computers and digital systems to record the number of events occurring in a specified interval of time.
- The combination of flip-flops that perform the counting operation are known as **Counters**.

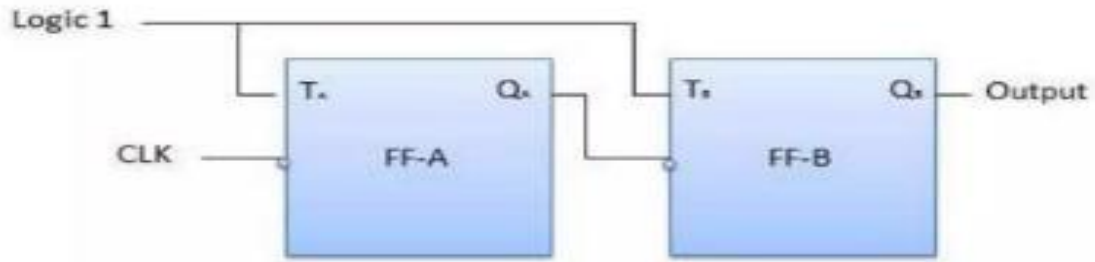
- Counters are classified into two categories according to the way they are clocked :
- **Asynchronous**/Ripple/Serial Counter
- **Synchronous**/Parallel Counter

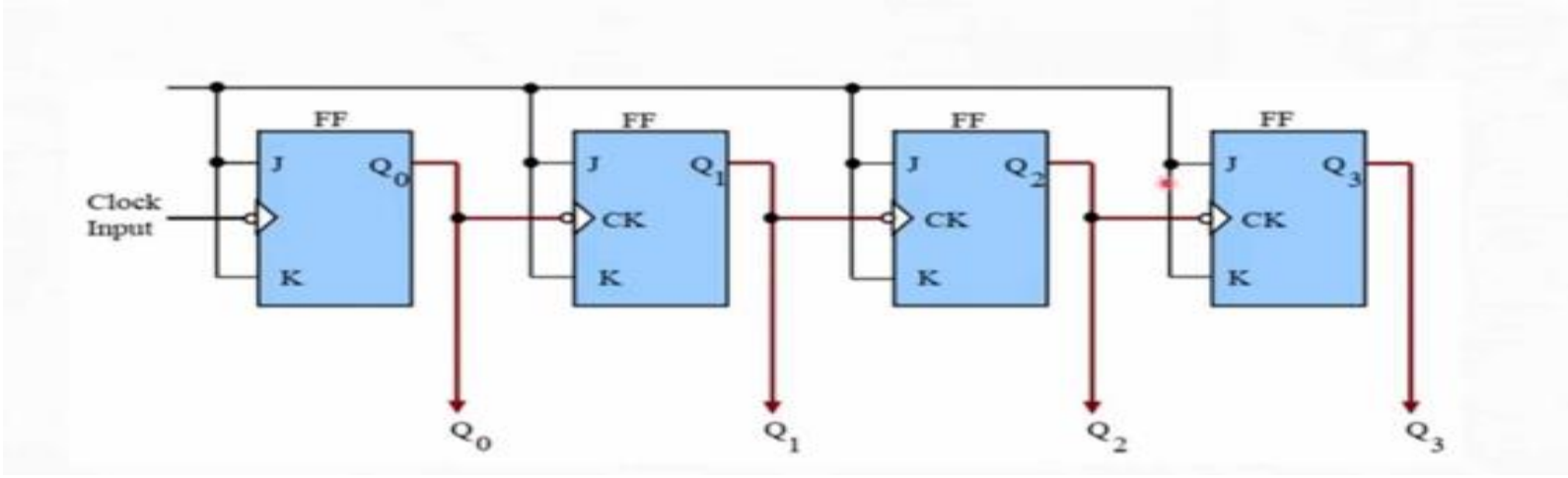
- Depending on the way in which the counting progresses, the synchronous or asynchronous counters are classified as follows –
- Up counters
- Down counters
- Up/Down counters

asynchronous counter

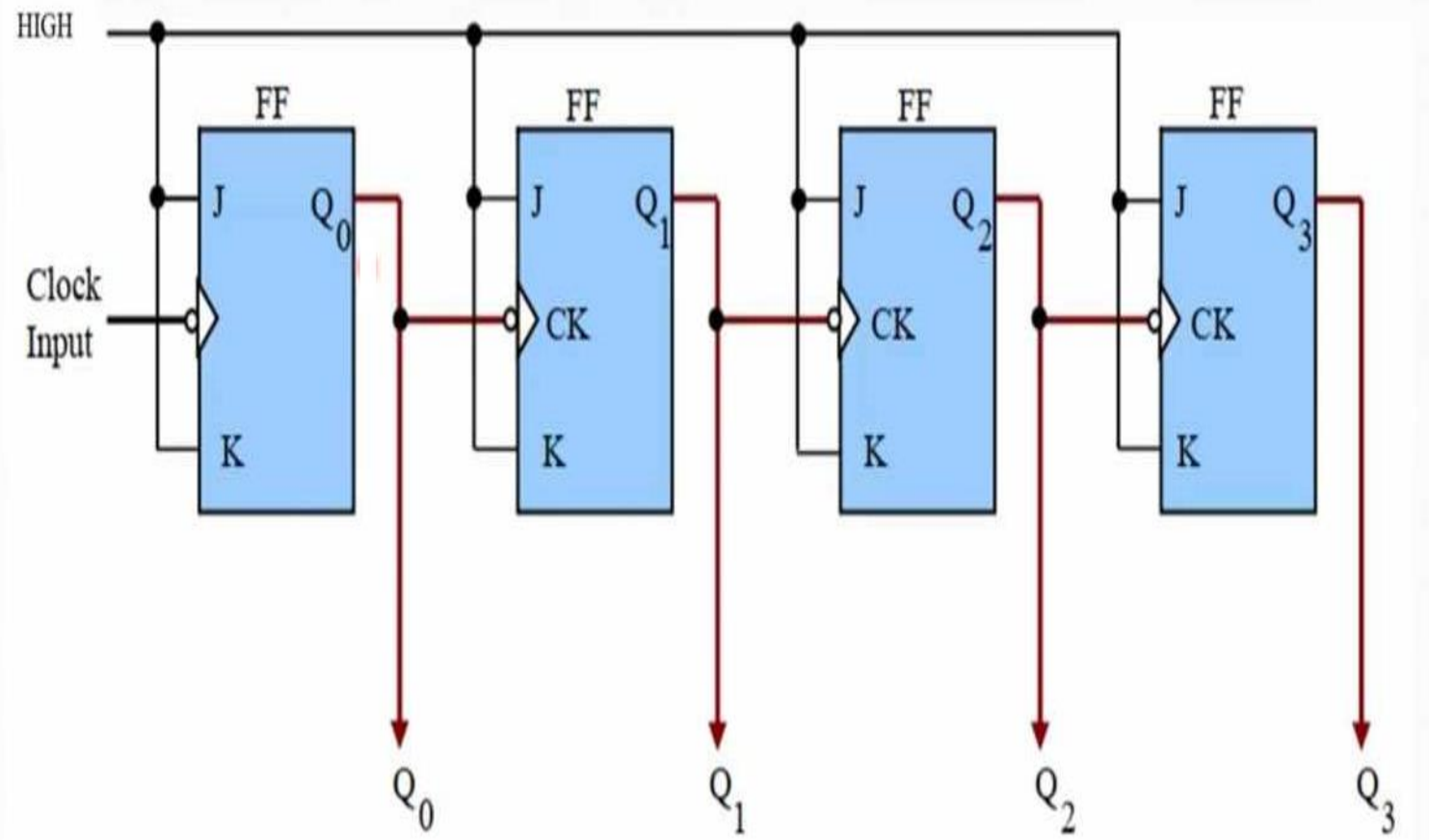
- In asynchronous counter we don't use universal clock, only first flip flop is driven by main clock and the clock input of rest of the following counters is driven by output of previous flip flops.
- An asynchronous counter is one in which the flip-flops (FF) within the counter do not change states at exactly the same time because they do not have a common clock pulse.

- We can understand it by following diagram

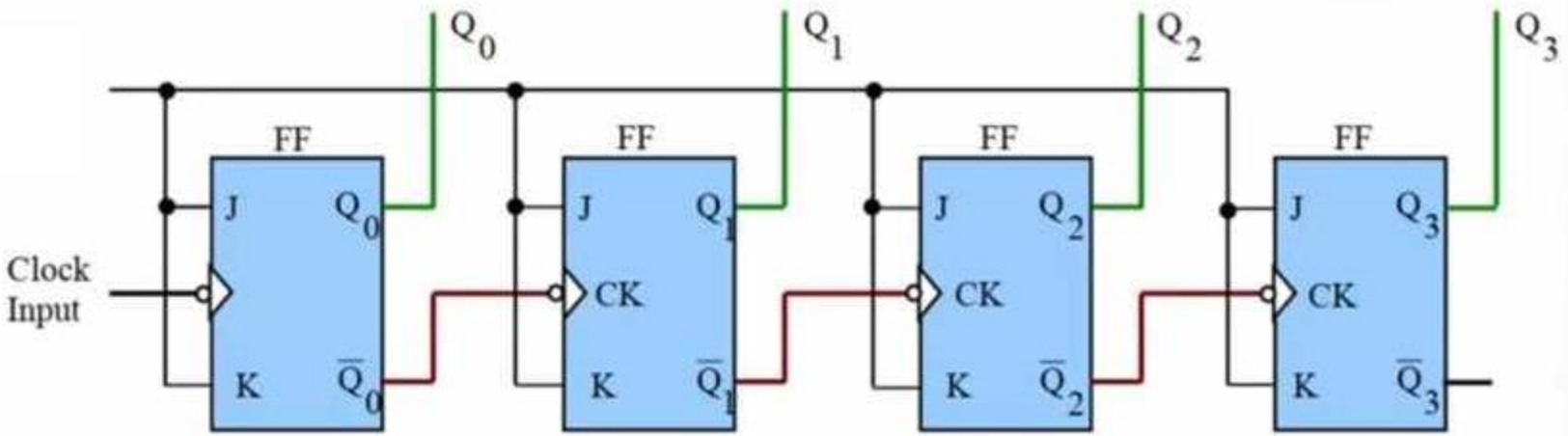




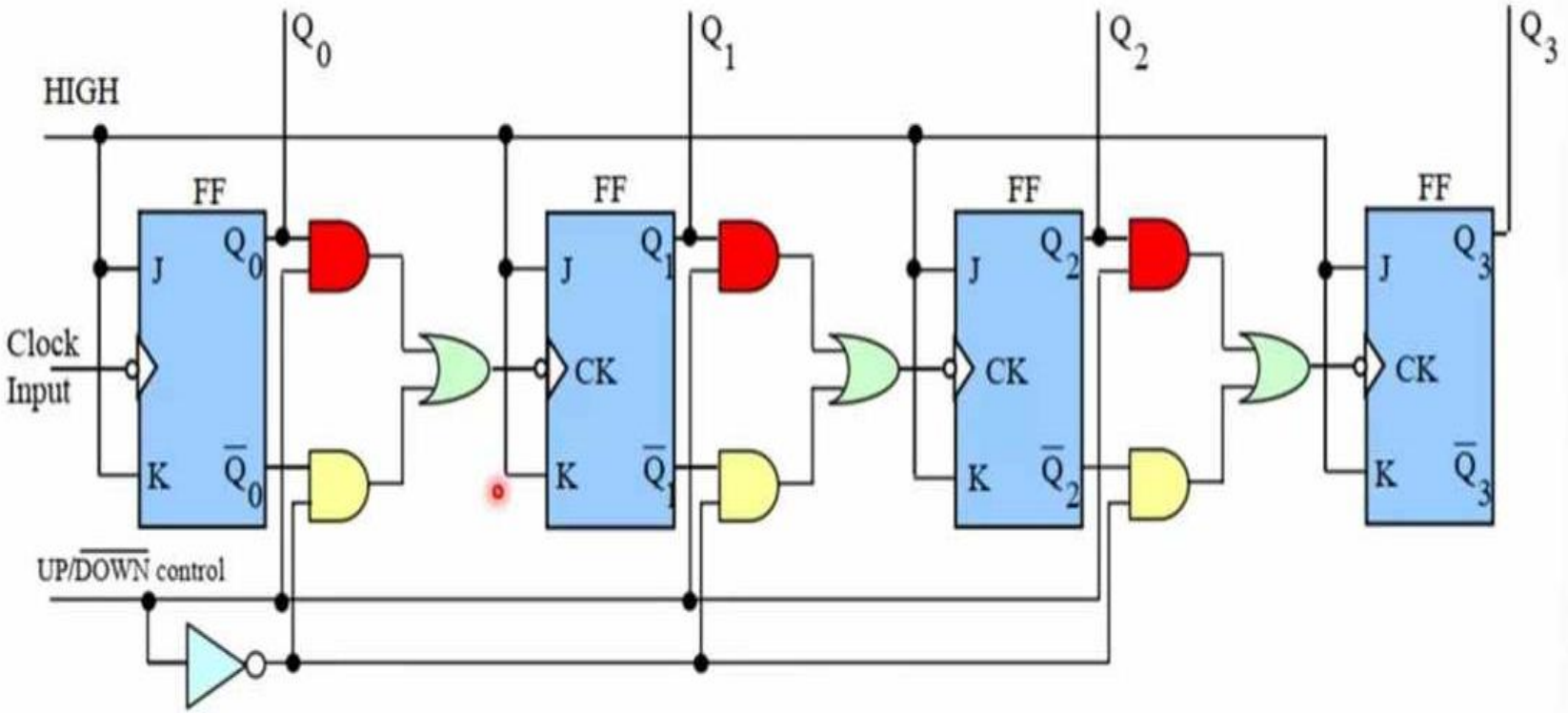
4 -bit asynchronous up conunter



4 bit asynchronous down counter



4 bit asynchronous up/down counter



Modulo-n Counters

Counters are often required which count up to a desired number value then reset to „0" and start counting again from the beginning or stop and wait for a new start signal. The modulo-10 counter is used most frequently for displaying BCD numbers in dual code. This is a 4-bit dual counter with only 10 numeric values. It counts up to "9" and then starts again at „0". Consequently there is always a dual number in 8421-BCD code at the outputs. 8421-BCD counters are also known as **decimal counters**. The functional principle of a modulo-10 counter is that a 4-bit dual counter is reset at the instant at which the counter switches to 1010. After switching, the reset signal must become inactive (passive) immediately so that the counting process can be continued with the value 0000.

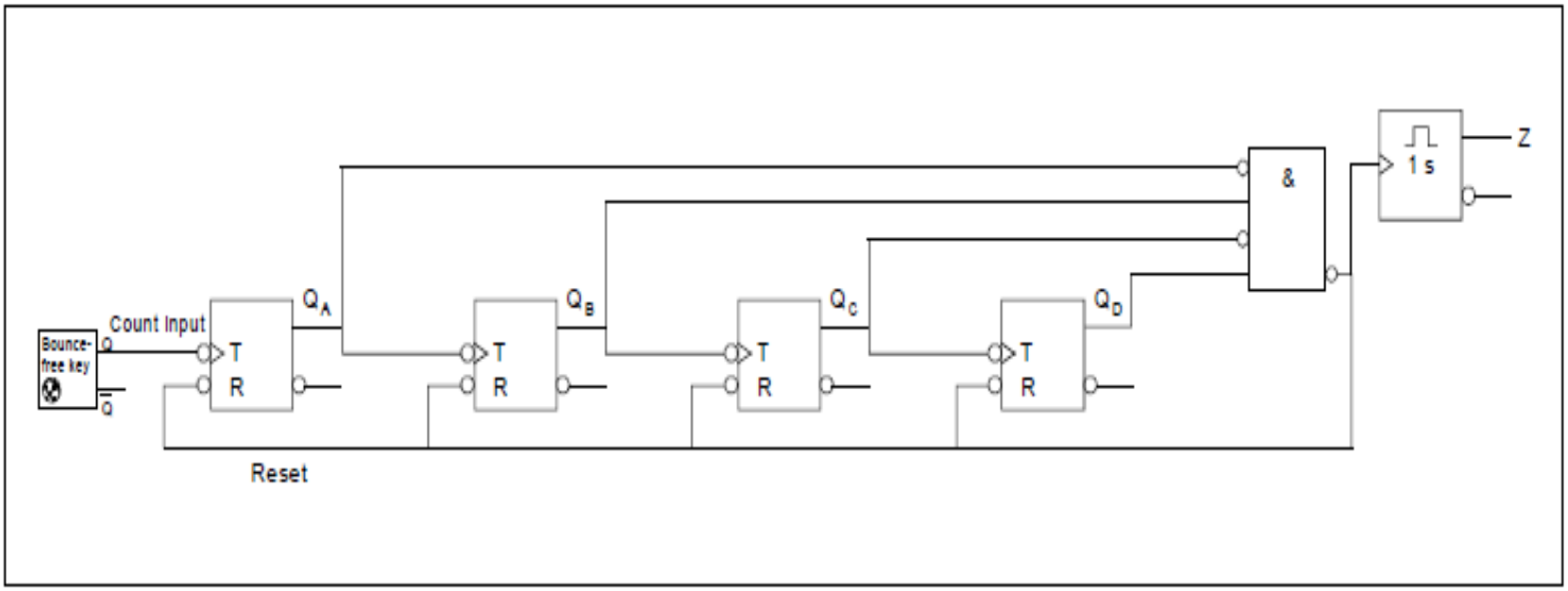


Fig. 7.2.4.1 Modulo-10 counter with practical application

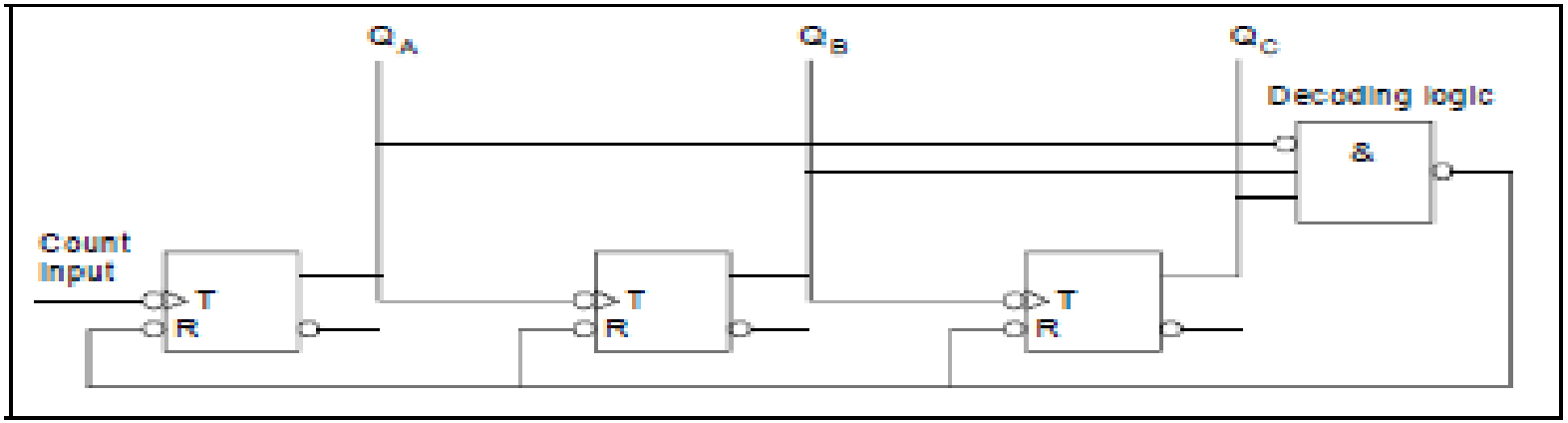


Fig. 7.1.4.1 Asynchronous modulo-6 counter

Asynchronous counter IC

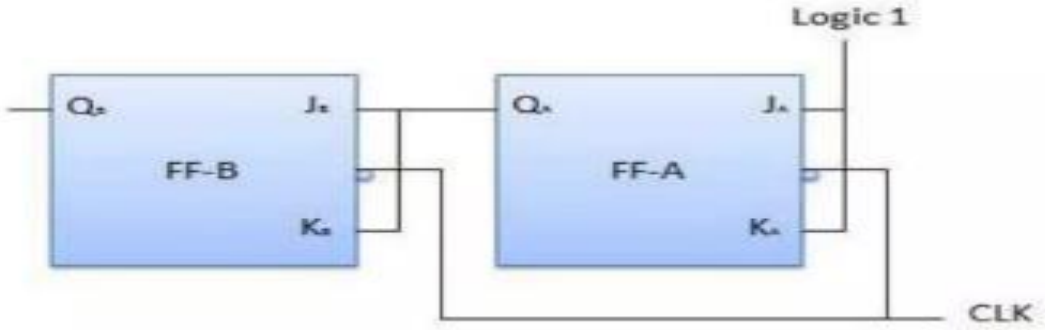
74LS90, Decade Counter
74LS92, Divide by 12 Counter
74LS93, 4-bit binary counter
74LS290/74LS196, Decade counter (MOD 10)
74LS293/74LS197, binary counter (MOD 16)
74LS390 Dual decade counter
74LS393 Dual 4-bit counter

Synchronous Counter

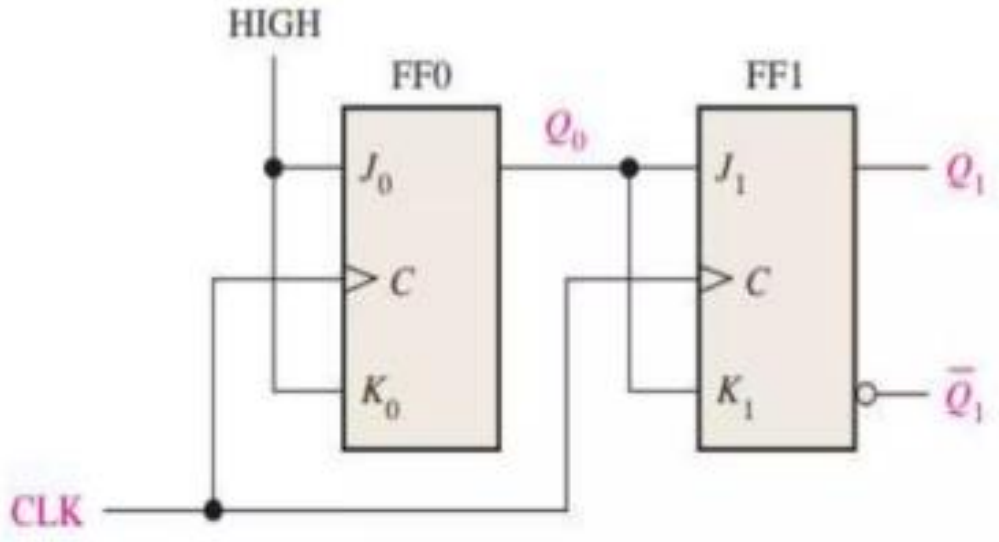
- If the "clock" pulses are applied to all the flip-flops in a counter simultaneously, then such a counter is called as synchronous counter.
- Unlike the asynchronous counter, synchronous counter has one global clock which drives each flip flop so output changes in parallel.
- The one advantage of synchronous counter over asynchronous counter is, it can operate on higher frequency than asynchronous counter as it does not have cumulative delay because of same clock is given to each flip flop.

- synchronous counter is one in which all the flip-flops in the counter are clocked at the same time by a common clock pulse.
- J-K flip-flops are used to illustrate most synchronous counters.
- D flip-flops can also be used but generally require more logic because of having no direct toggle or no-change states

- We can understand it by following diagram



2-Bit Synchronous Binary Counter



(a) J-K flip-flop

Operation

- The operation of a J-K flip-flop synchronous counter is as follows: First, assume that the counter is initially in the binary 0 state; that is, both flip-flops are RESET. When the positive edge of the first clock pulse is applied, FF0 will toggle and Q0 will therefore go HIGH. What happens to FF1 at the positive-going edge of CLK1? To find out, let's look at the input conditions of FF1. Inputs J1 and K1 are both LOW because Q0, to which they are connected, has not yet gone HIGH. Remember, there is a propagation delay from the triggering edge of the clock pulse until the Q output actually makes a transition. So, J = 0 and K = 0 when the leading edge of the first clock pulse is applied. This is a no-change condition, and therefore FF1 does not change state

After CLK1, $Q_0 = 1$ and $Q_1 = 0$ (which is the binary 1 state). When the leading edge of CLK2 occurs, FF0 will toggle and Q_0 will go LOW. Since FF1 has a HIGH ($Q_0 = 1$) on its J_1 and K_1 inputs at the triggering edge of this clock pulse, the flip-flop toggles and Q_1 goes HIGH. Thus, after CLK2, $Q_0 = 0$ and $Q_1 = 1$ (which is a binary 2 state).

When the leading edge of CLK3 occurs, FF0 again toggles to the SET state ($Q_0 = 1$), and FF1 remains SET ($Q_1 = 1$) because its J_1 and K_1 inputs are both LOW ($Q_0 = 0$). After this triggering edge, $Q_0 = 1$ and $Q_1 = 1$ (which is a binary 3 state).

Finally, at the leading edge of CLK4, Q_0 and Q_1 go LOW because they both have a toggle condition on their J and K inputs.

The complete timing diagram for the counters is shown in Figure 9–14.

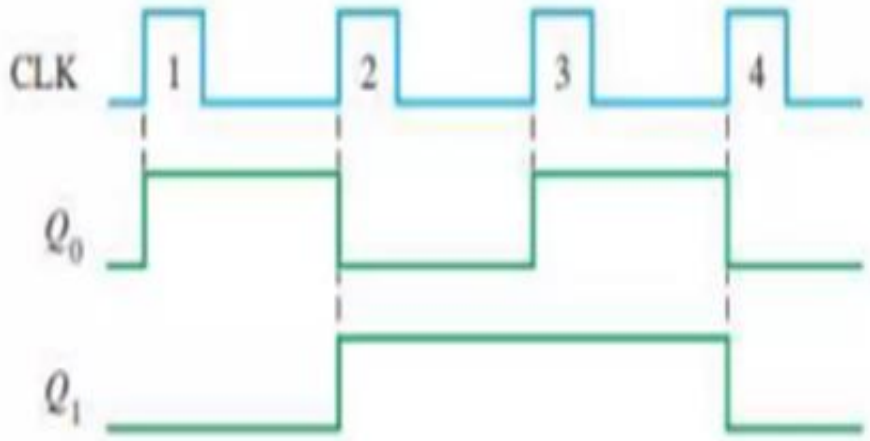
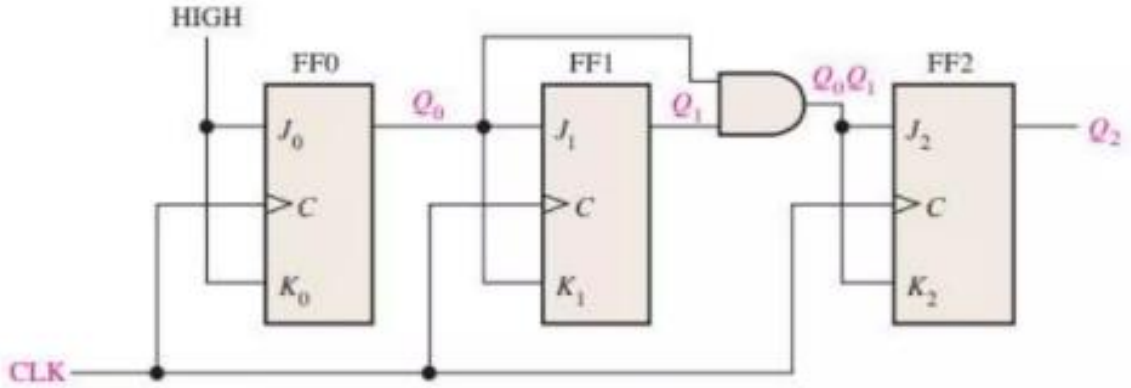
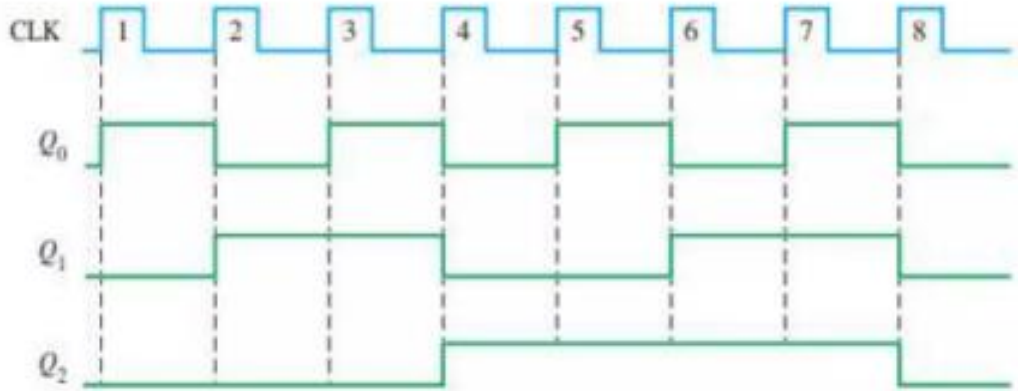


FIGURE 9–14 Timing diagram for the counters

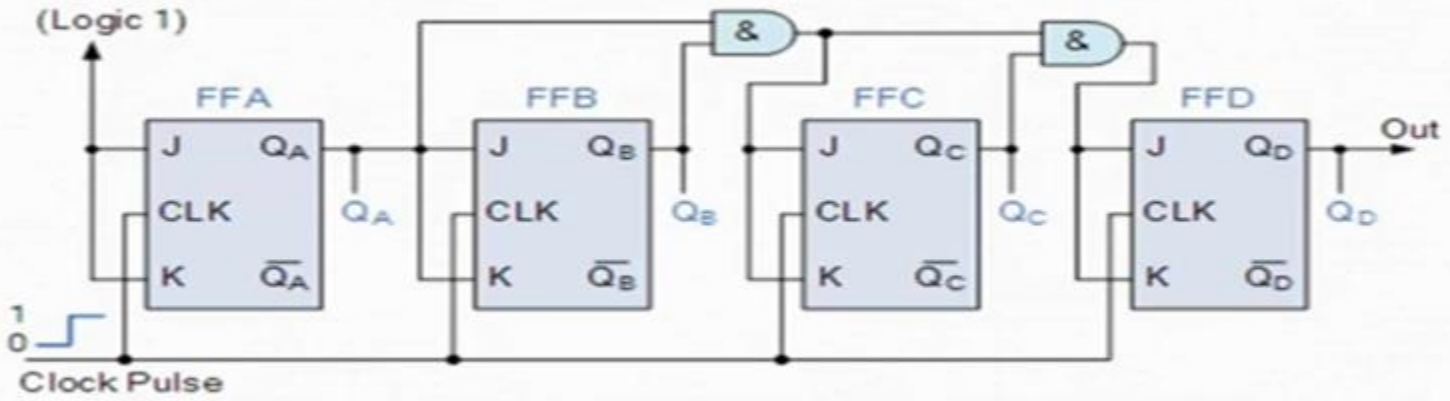
3-Bit Synchronous Binary Counter



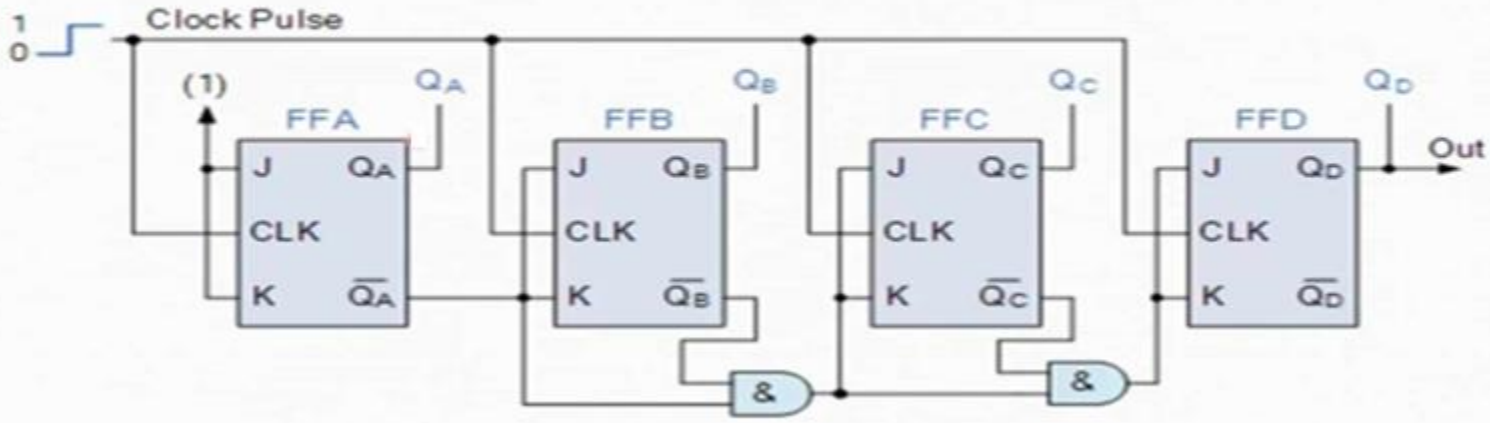
Timing Diagram



Binary 4-bit Synchronous Up Counter



Binary 4-bit Synchronous Down Counter



synchronous counters IC

TTL 74LS193 or CMOS CD4510 are 4-bit binary Up or Down counters

74HC190 4-bit BCD decade Up/Down counter, the 74F569 is a fully synchronous Up/Down binary counter and the CMOS 4029 4-bit Synchronous Up/Down counter.

The 74LS160A/162A are BCD synchronous counters
The 74LS161A/163A are binary 4-bit synchronous counters