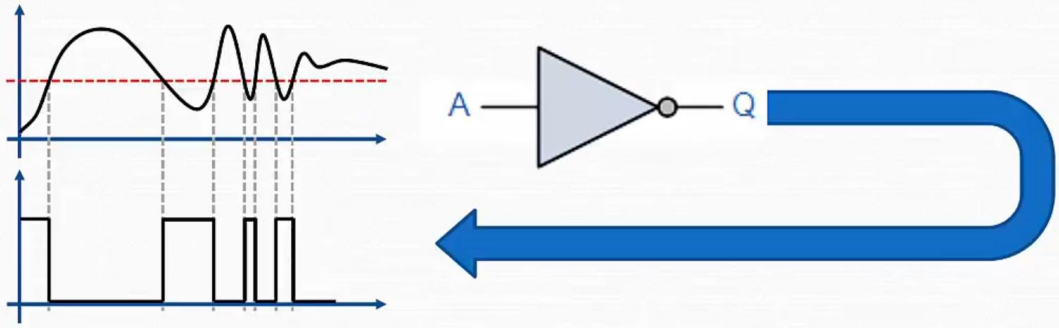
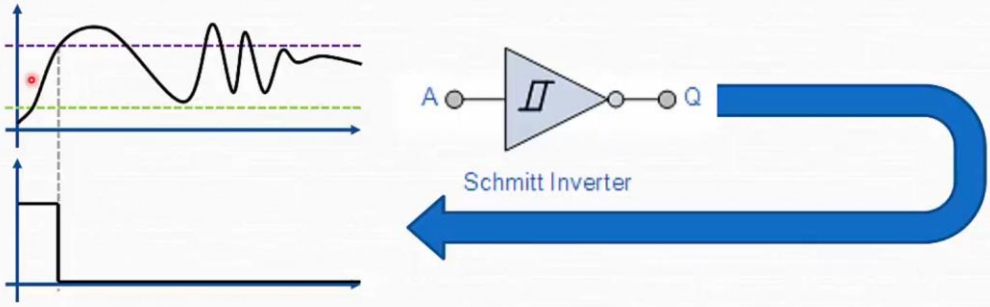
Schmitt Inverter (NOT Gate)

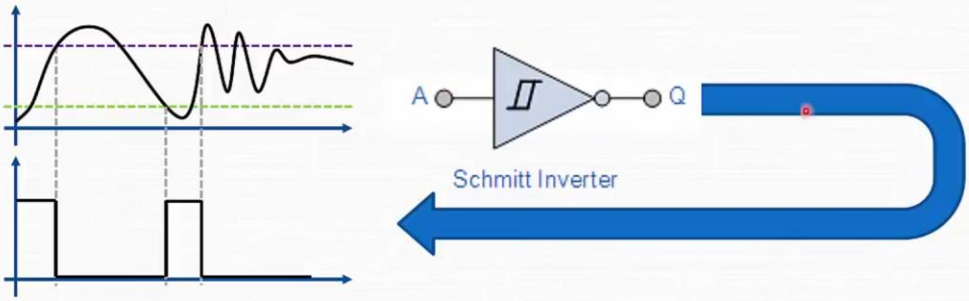


Schmitt Inverter (NOT Gate)



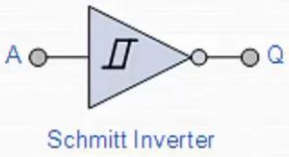
بكل بساطة في اي شيء يسمى شميت (**Schmitt**) يجب ان تتجاوز الاشارة قيمتين فاصلتين لتحدث اي تغيير

Schmitt Inverter (NOT Gate)

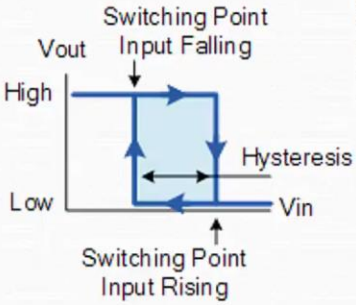


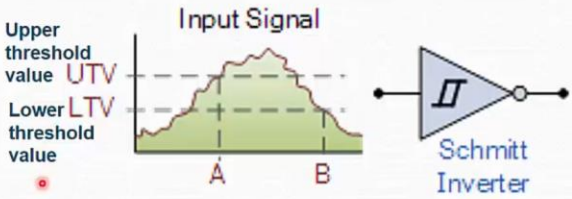
بكل بساطة في اي شيء يسمى شميت (**Schmitt**) يجب ان تتجاوز الاشارة قيمتين فاصلتين لتحدث اي تغيير

Schmitt Inverter (NOT Gate)



Schmitt Inverter



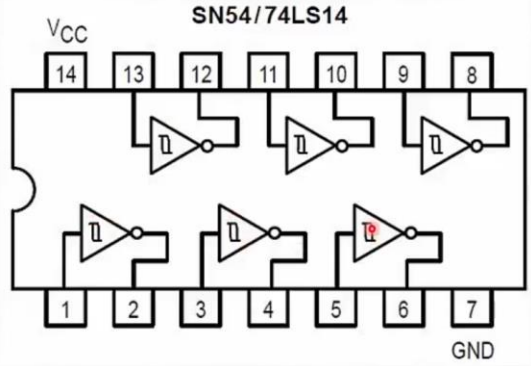


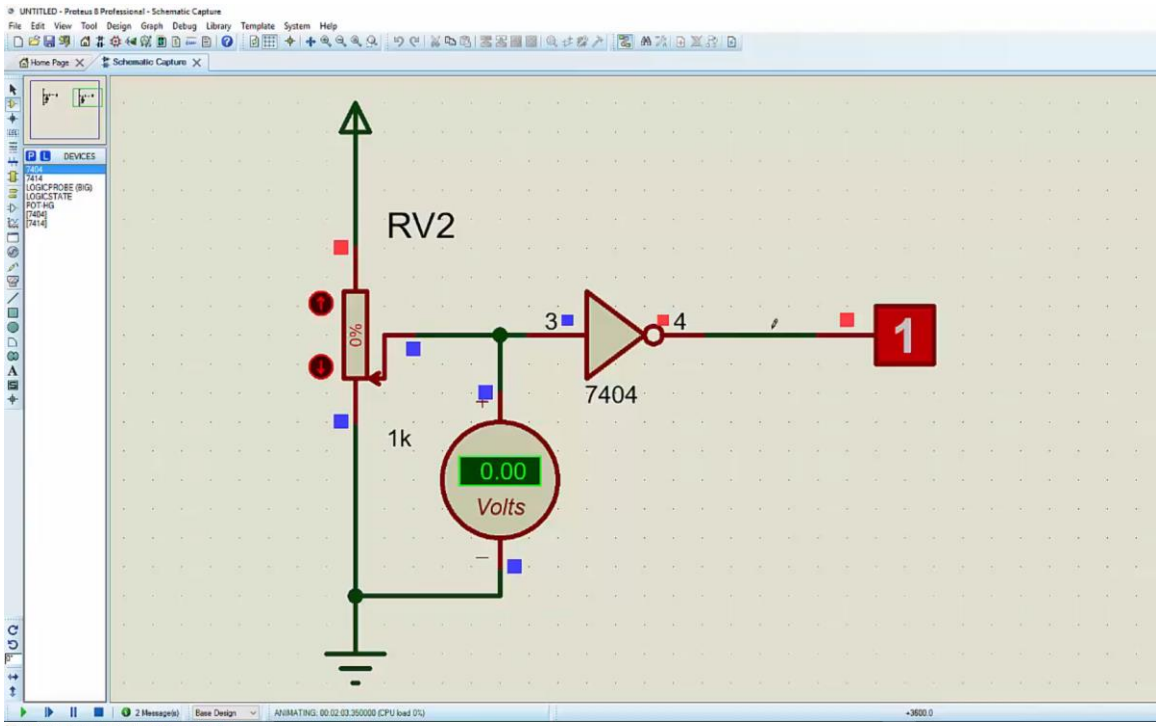
TTL Logic Types

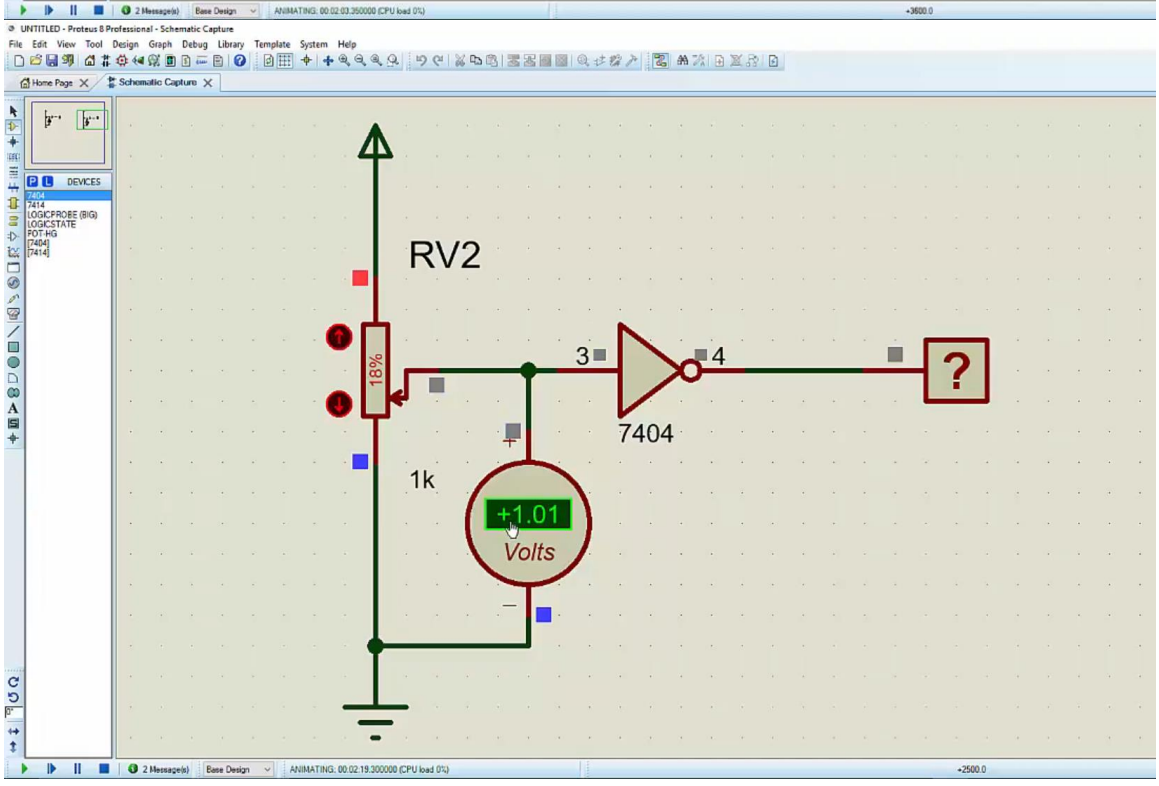
74LS14 Hex Schmitt Inverting NOT Gate

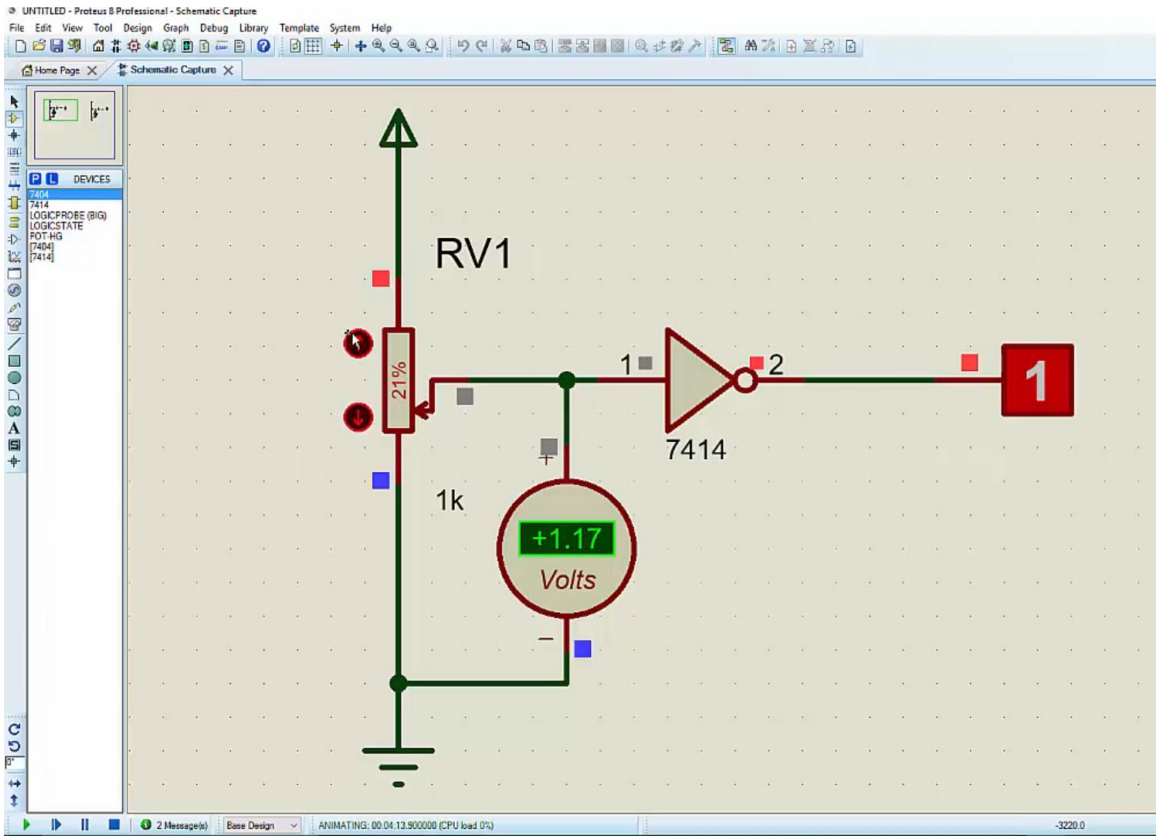
CMOS Logic Types

CD40106 Hex Schmitt Inverting NOT Gate




UNTITLED - Proteus 8 Professional - Schematic Capture
RV2
0%
1k
3
4
7404
1
0.00
Volts


UNTITLED - Proteus 8 Professional - Schematic Capture
RV2
18%
1k
3
4
7404
?
+1.01
Volts



TEXAS INSTRUMENTS

SN5414, SN54LS14, SN7414, SN74LS14
SDLS049C – DECEMBER 1983 – REVISED NOVEMBER 2016

SNx414 and SNx4LS14 Hex Schmitt-Trigger Inverters

1 Features

- Operation From Very Slow Edges
- Improved Line-Receiving Characteristics
- High Noise Immunity

2 Applications

- HVAC Gateways
- Residential Ductless Air Conditioning Outdoor Units
- Robotic Controls
- Industrial Stepper Motors
- Power Meter and Power Analyzers
- Digital Input Modules for Factory Automation

3 Description

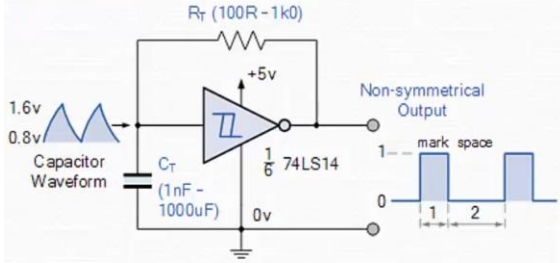
Each circuit in SNx414 and SNx4LS14 functions as an inverter. However, because of the Schmitt-Trigger action, they have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

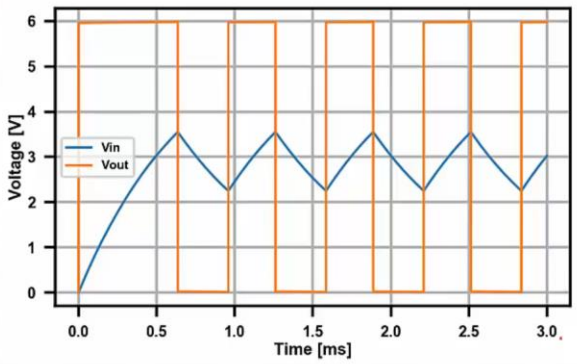
Device Information(1)

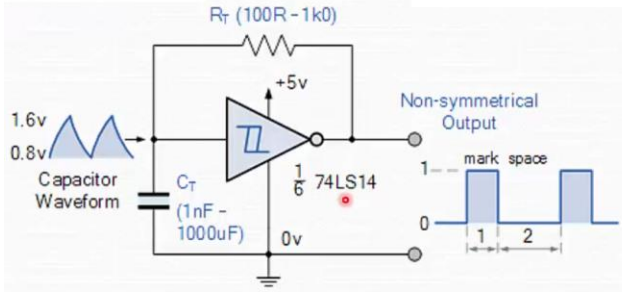
PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN7414, SN74LS14	SOIC (14)	4.90 mm × 3.91 mm
	SSOP (14)	6.20 mm × 5.30 mm
	PDIP (14)	19.30 mm × 6.35 mm
	SO (14)	10.30 mm × 5.30 mm
SN5414, SN54LS14	CDIP (14)	19.56 mm × 6.67 mm
	CFP (14)	9.21 mm × 5.97 mm
	LCCC (20)	8.89 mm × 8.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

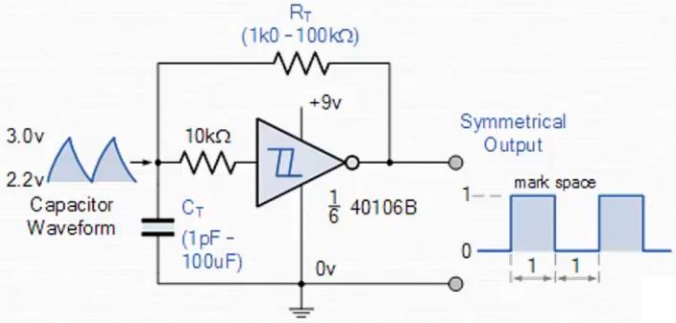


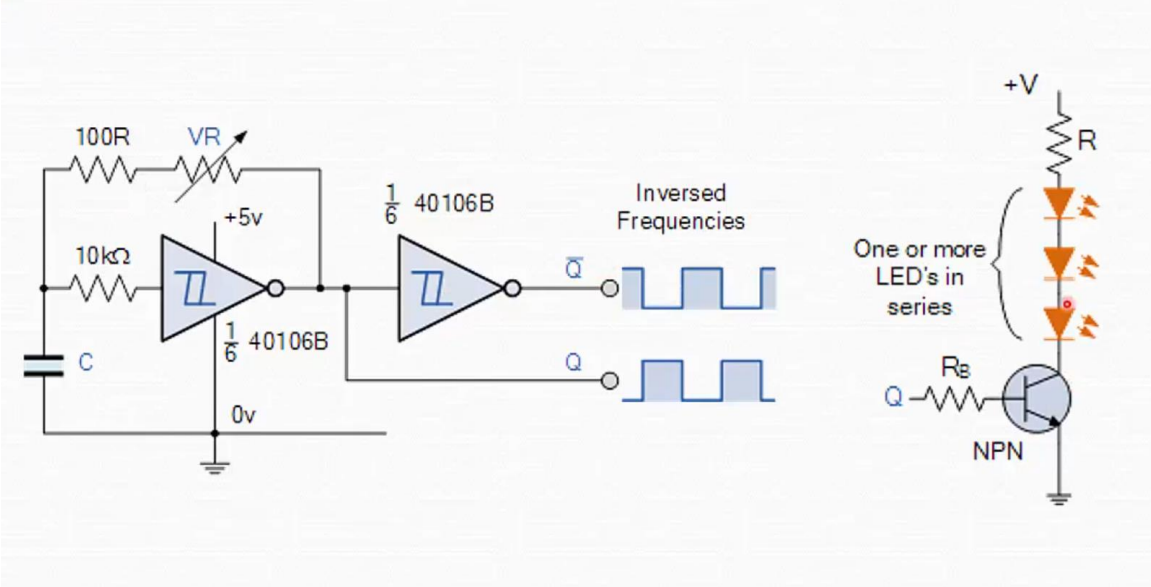
$$f = \frac{1}{1.2RC}$$

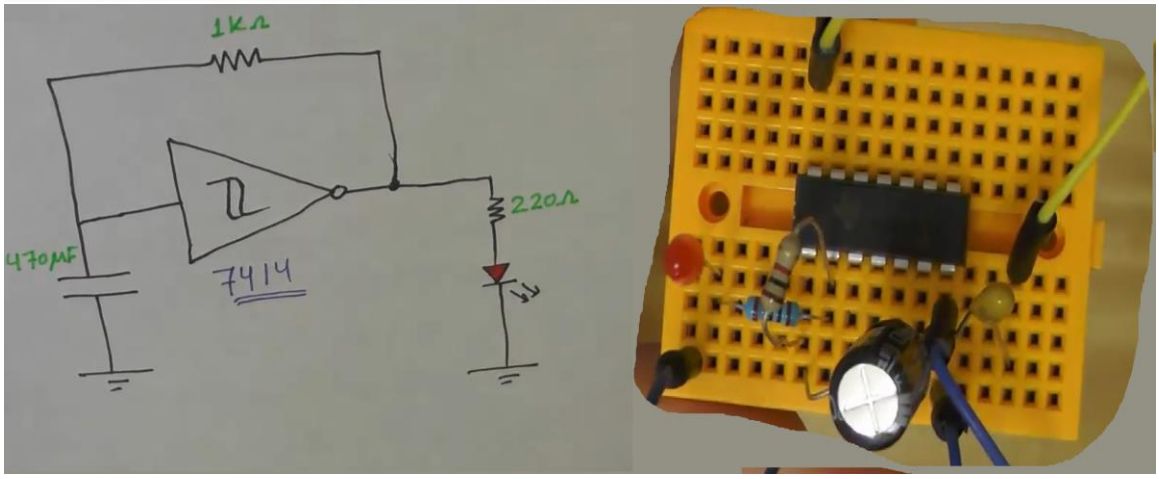




$$f = \frac{1}{1.2RC}$$



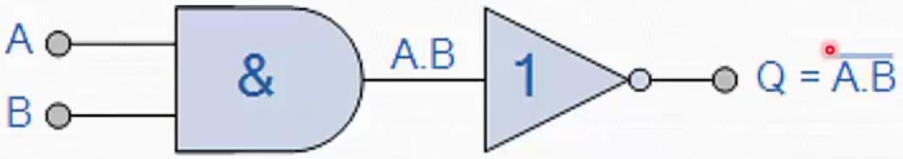

100R
VR
+5v
10kΩ
C
1/6 40106B
1/6 40106B
Inversed Frequencies
Q̄
Q
0v
+V
R
One or more LED's in series
RB
Q
NPN


1kΩ
220Ω
470μF
7414

البوابات المنطقية

NAND

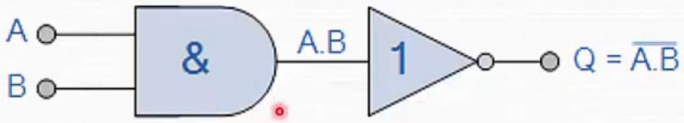
NOT AND



2-input "AND" gate plus a "NOT" gate

البوابات المنطقية

بوابة NAND

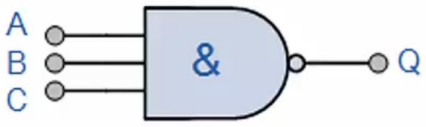


2-input "AND" gate plus a "NOT" gate

Symbol	Truth Table		
	B	A	Q
	0	0	1
	0	1	1
	1	0	1
	1	1	0
Boolean Expression **Q = $\overline{A.B}$**	Read as A **AND** B gives **NOT** Q		

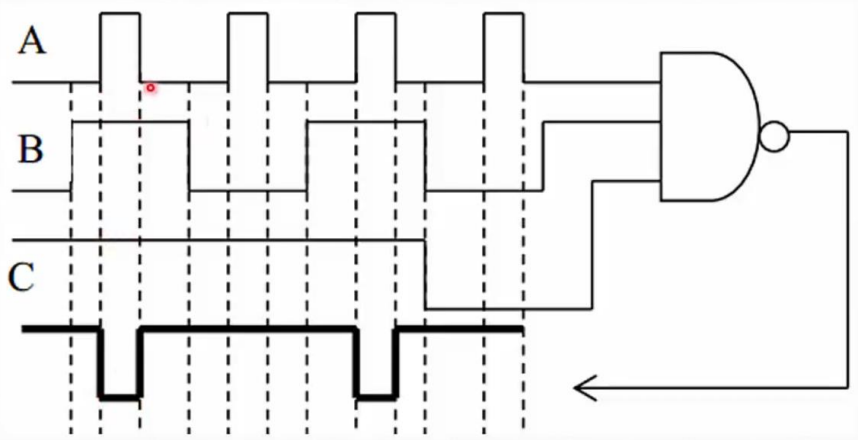
2-input NAND Gate

ذات ثلاث مداخل

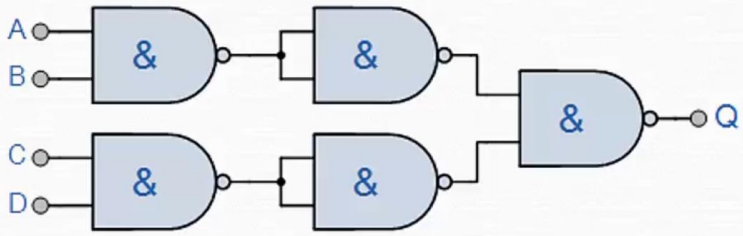
Symbol	Truth Table			
	C	B	A	Q
	0	0	0	1
	0	0	1	1
	0	1	0	1
	0	1	1	1
	1	0	0	1
	1	0	1	1
	1	1	0	1
	1	1	1	0
Boolean Expression **Q = $\overline{A.B.C}$**	Read as A **AND** B **AND** C gives **NOT** Q			

3-input NAND Gate

القاعدة السهلة / أي صفر على أي دخل ..... يخرج واحد



بوابة NAND بأربعة مداخل من بوابات ذات مدخلين

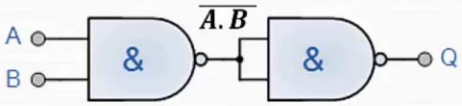


$$Q = \overline{A.B.C.D}$$

ملاحظة اذا كان هناك مدخل زائد عن الحاجة يجب ربطه بـ 5 فولت (Logic 1) أوربطه بمدخل آخر (أي دمج مدخلين مع بعض)

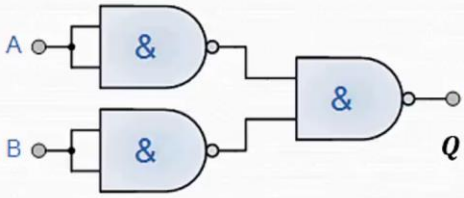
بوابة NAND لاستعمالات متعددة

NOT Gate



2-input AND Gate

$$Q = \overline{\overline{A.B}} = A.B$$



$$Q = \overline{\overline{A}.\overline{B}} = A + B$$

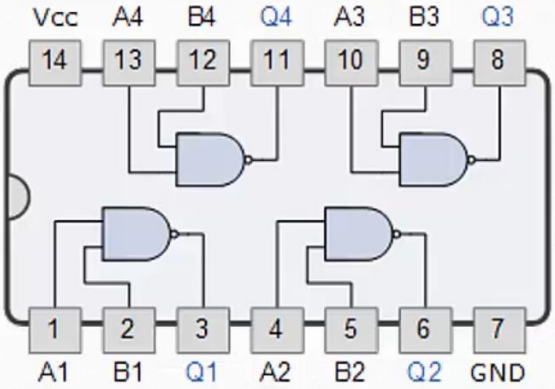
2-input OR Gate

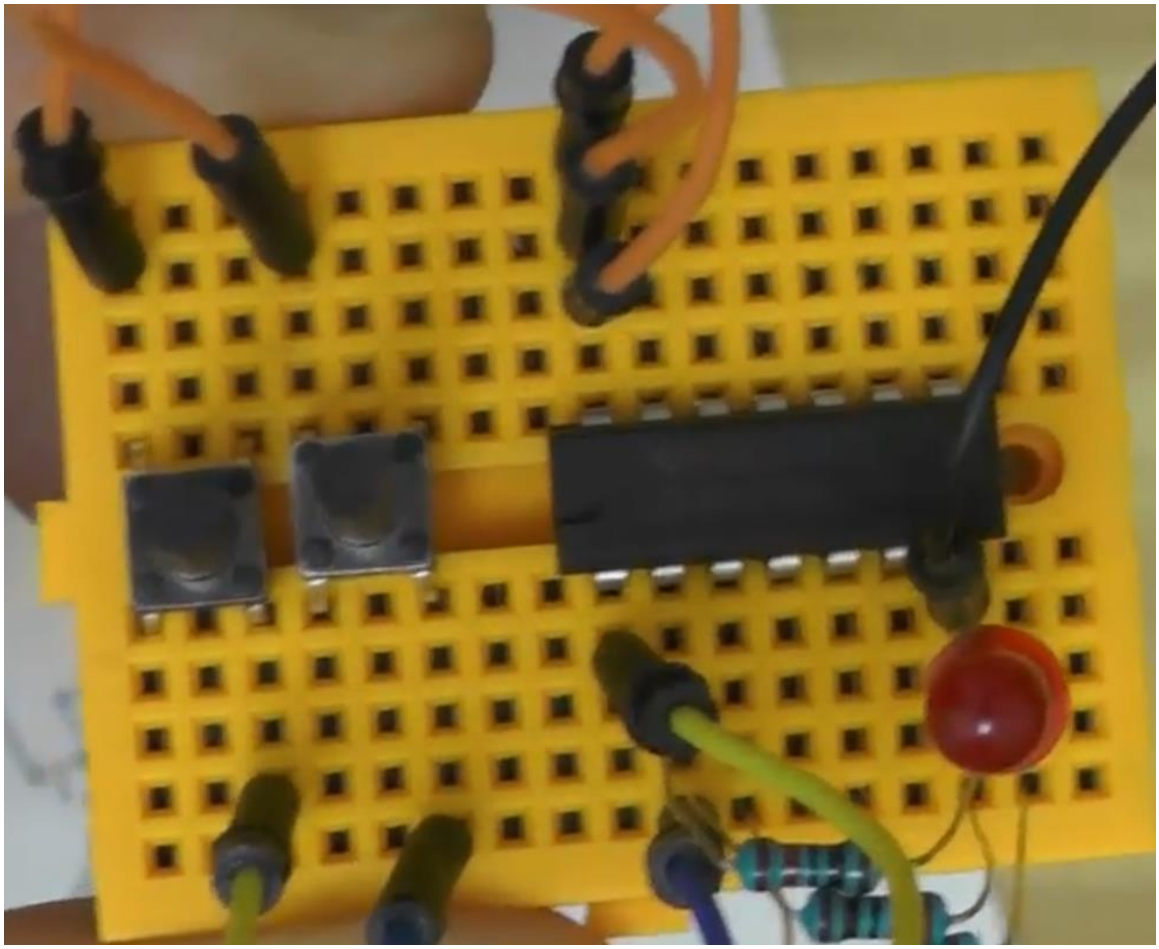
TTL Logic Types

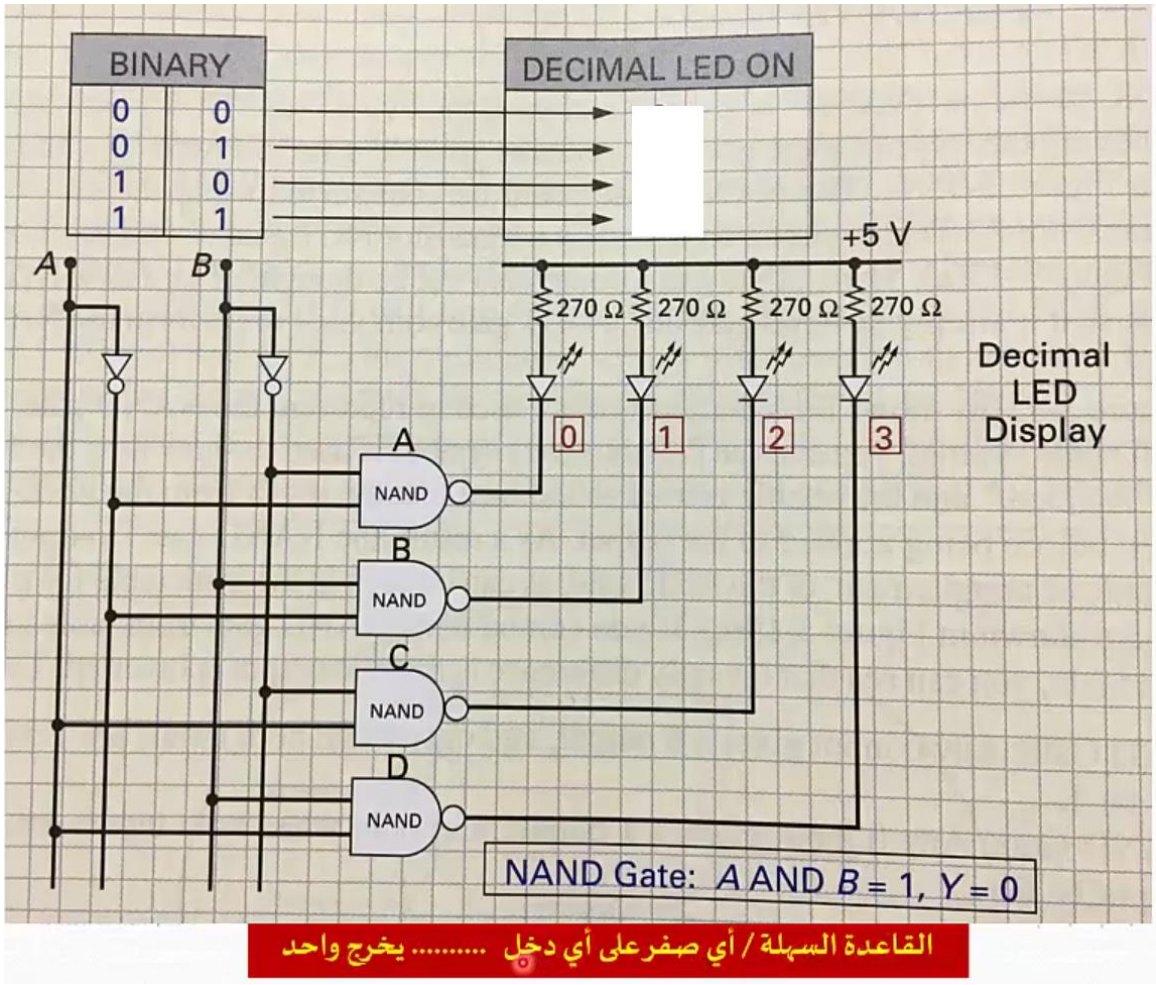
74LS00 Quad 2-input
74LS10 Triple 3-input
74LS20 Dual 4-input
74LS30 Single 8-input

CMOS Logic Types

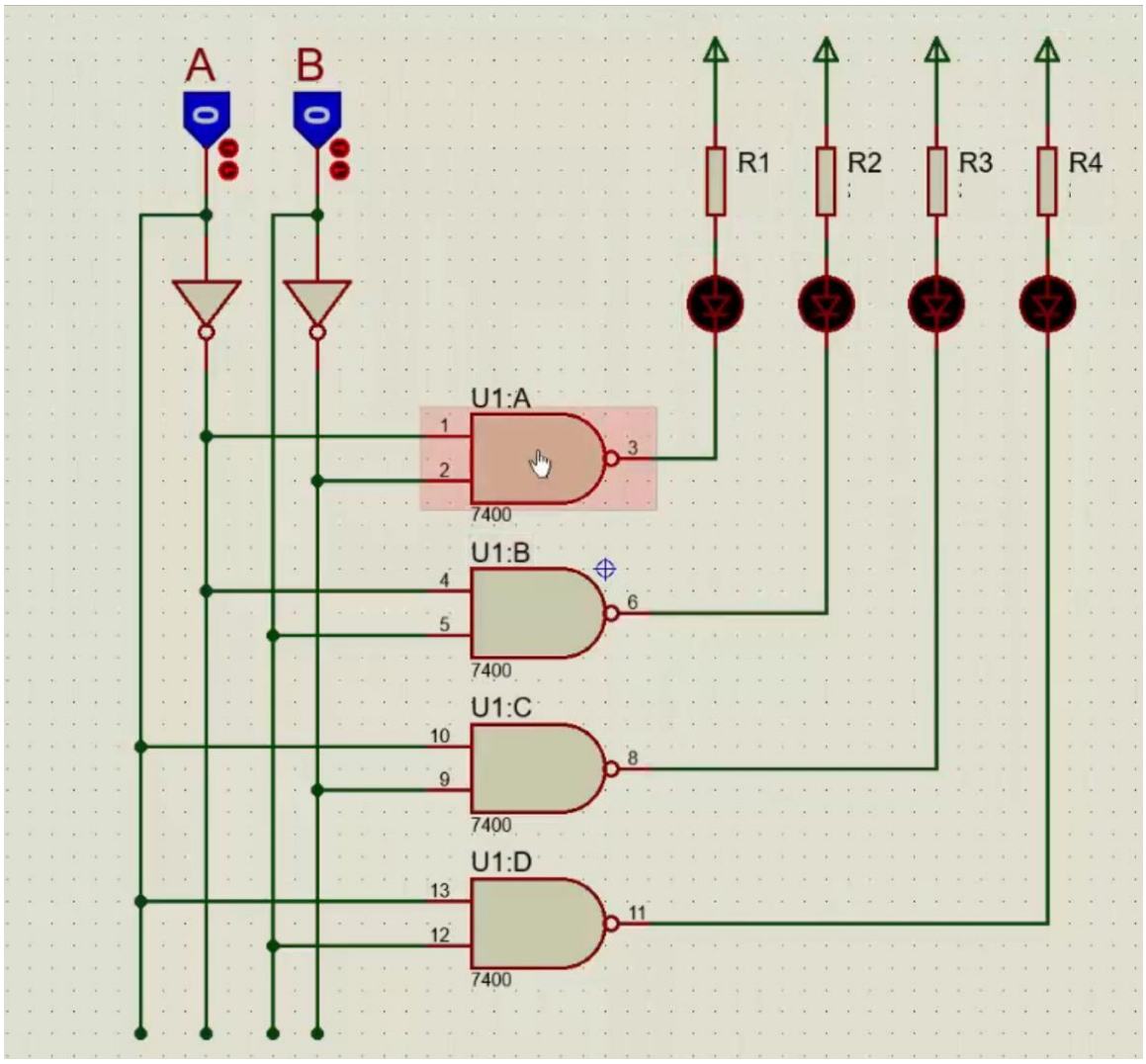
CD4011 Quad 2-input
CD4023 Triple 3-input
CD4012 Dual 4-input



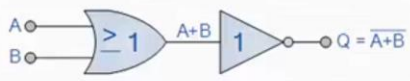




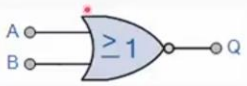
القاعدة السهلة / أي صفر على أي دخل ..... يخرج واحد

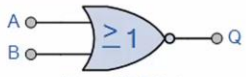

A
B
R1
R2
R3
R4
U1:A
1
2
3
7400
U1:B
4
5
6
7400
U1:C
10
9
8
7400
U1:D
13
12
11
7400

بوابة NOR

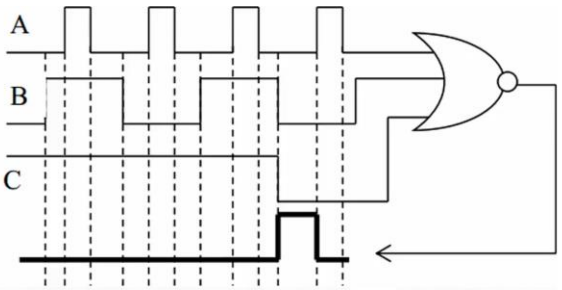


2-input "OR" gate plus a "NOT" gate

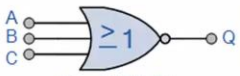


Symbol	Truth Table		
 2-input NOR Gate	B	A	Q
	0	0	1
	0	1	0
	1	0	0
	1	1	0
Boolean Expression $Q = \overline{A+B}$	Read as A **OR** B gives **NOT** Q		

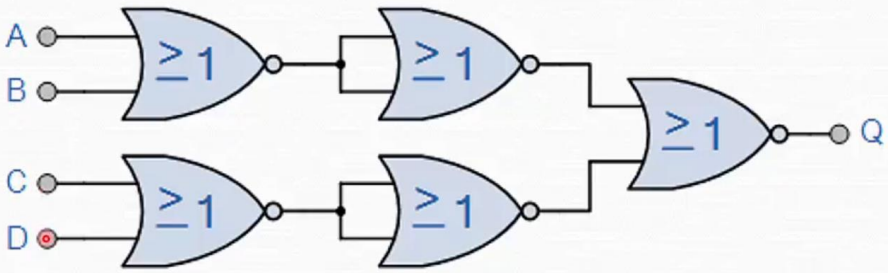
القاعدة السهلة / أي واحد على أي دخل ..... يخرج صفر



ذات ثلاث مداخل

Symbol	Truth Table			
 3-input NOR Gate	C	B	A	Q
	0	0	0	1
	0	0	1	0
	0	1	0	0
	0	1	1	0
	1	0	0	0
	1	0	1	0
	1	1	0	0
	1	1	1	0
Boolean Expression $Q = \overline{A+B+C}$	Read as A **OR** B **OR** C gives **NOT** Q			

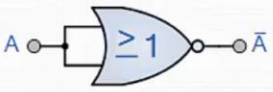
بوابة NOR بأربعة مداخل من بوابات ذات مدخلين

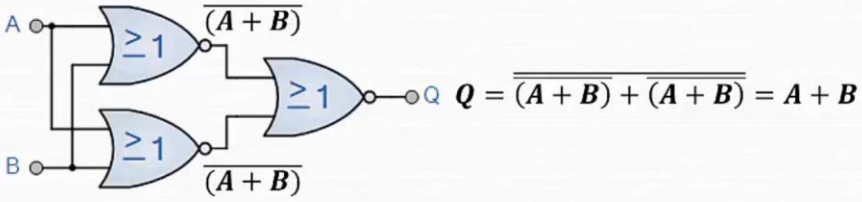


$$Q = \overline{A + B + C + D}$$

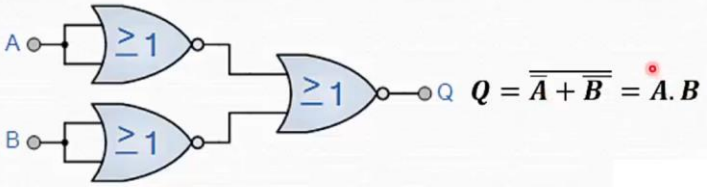
ملاحظة اذا كان هناك مدخل زائد عن الحاجة يجب ربطه بـ **0** فولت (**Logic 0**) أوربطه بمدخل آخر (أي دمج مدخلين مع بعض)

بوابة NOR لاستعمالات متعددة





$$Q = \overline{\overline{(A+B)} + \overline{(A+B)}} = A + B$$

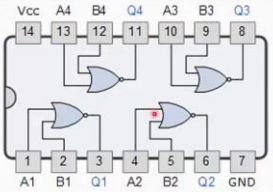


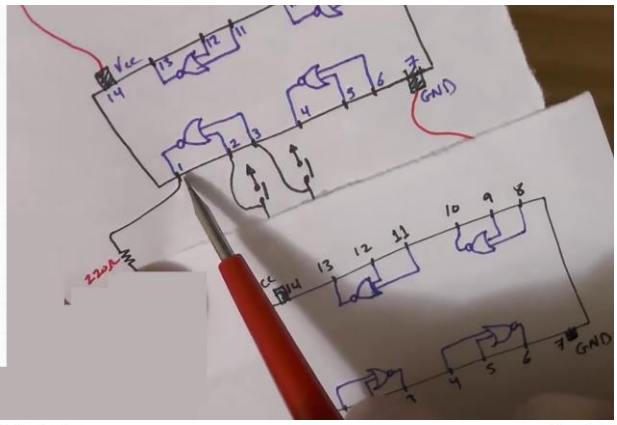
$$Q = \overline{\overline{A} + \overline{B}} = A.B$$

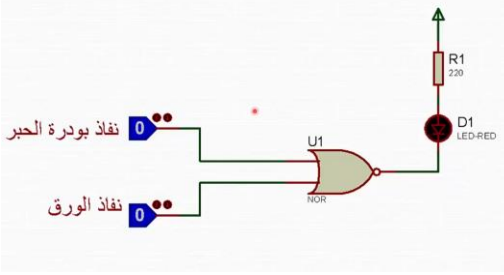
2-input AND Gate

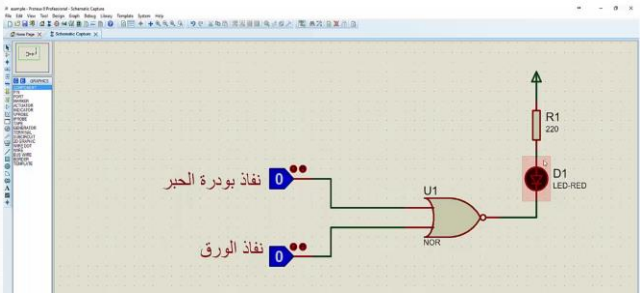
TTL Logic Types
74LS02 Quad 2-input
74LS27 Triple 3-input
74LS260 Dual 4-input

CMOS Logic Types
CD4001 Quad 2-input
CD4025 Triple 3-input
CD4002 Dual 4-input



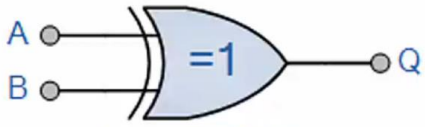






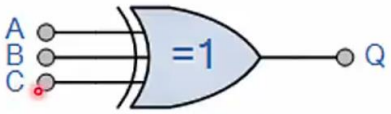
بوابة XOR بوابة Exclusive OR

بوابة عدم التكافؤ

Symbol	Truth Table		
 2-input Ex-OR Gate	B	A	Q
	0	0	0
	0	1	1
	1	0	1
	1	1	0
Boolean Expression Q = A ⊕ B	Read as A **OR** B but NOT **BOTH** gives Q		

$$Q = A \oplus B = \bar{A}.B + A.\bar{B}$$

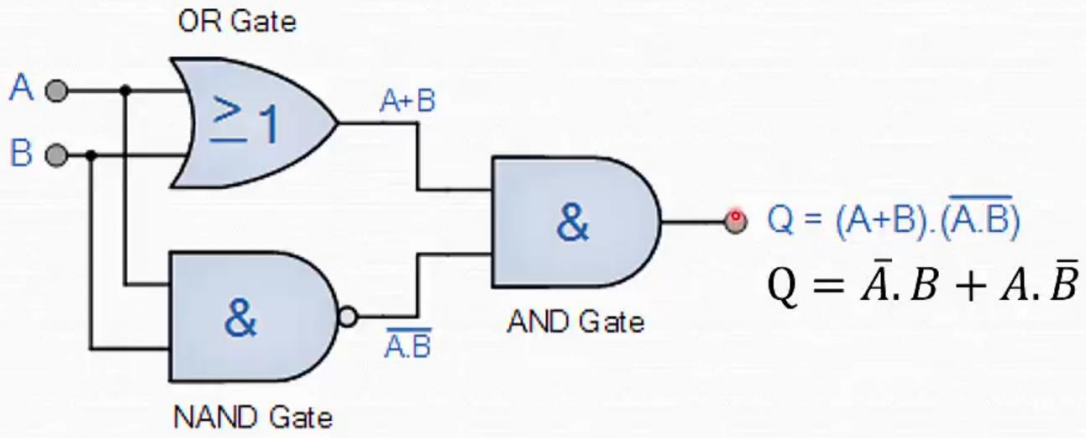
ذات ثلاث مداخل

Symbol	Truth Table			
 3-input Ex-OR Gate	C	B	A	Q
	0	0	0	0
	0	0	1	1
	0	1	0	1
	0	1	1	0
	1	0	0	1
	1	0	1	0
	1	1	0	0
	1	1	1	1
Boolean Expression Q = A ⊕ B ⊕ C	Read as "any **ODD** number of Inputs" gives Q			

يكون الخرج 1 عندما يكون هناك عدد فردي من المداخل 1

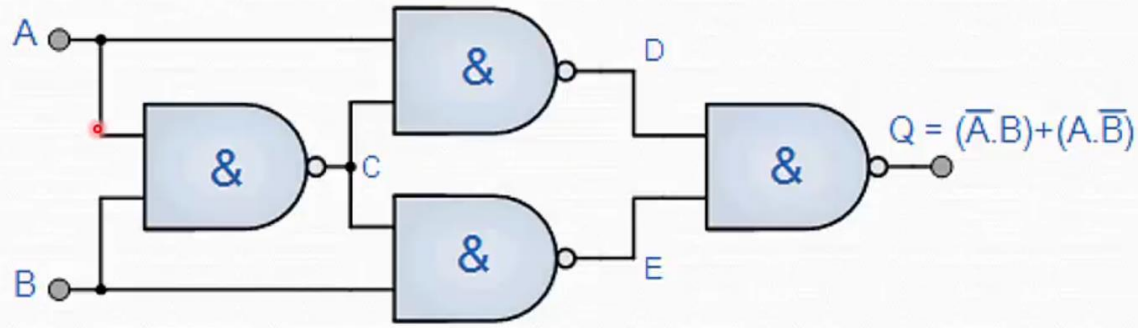
ملاحظة اذا كان هناك مدخل زائد عن الحاجة يجب ربطه بـ **0** فولت (**Logic 0**)
هنا **خطأ كبير** لو تم ربطه بمدخل آخر (أي دمج مدخلين مع بعض)

XOR من البوابات الرئيسية



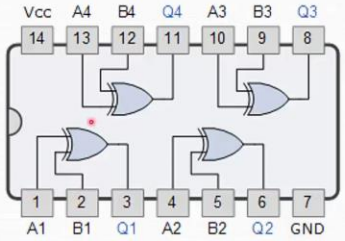
$$Q = \bar{A}.B + A.\bar{B}$$

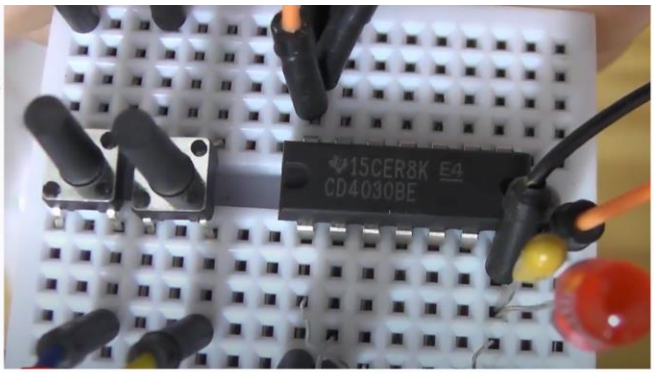
XOR من بوابة NAND

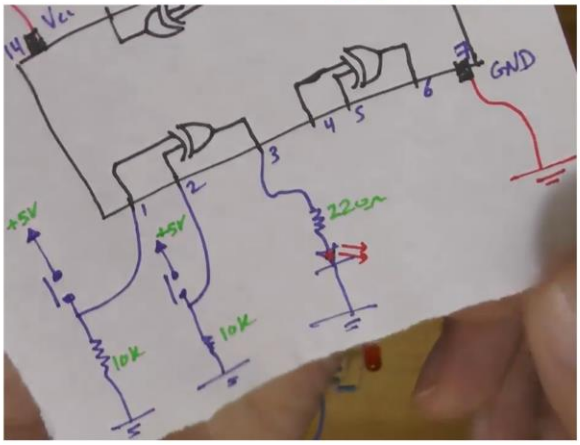


TTL Logic Types
74LS86 Quad 2-input

CMOS Logic Types
CD4030 Quad 2-input

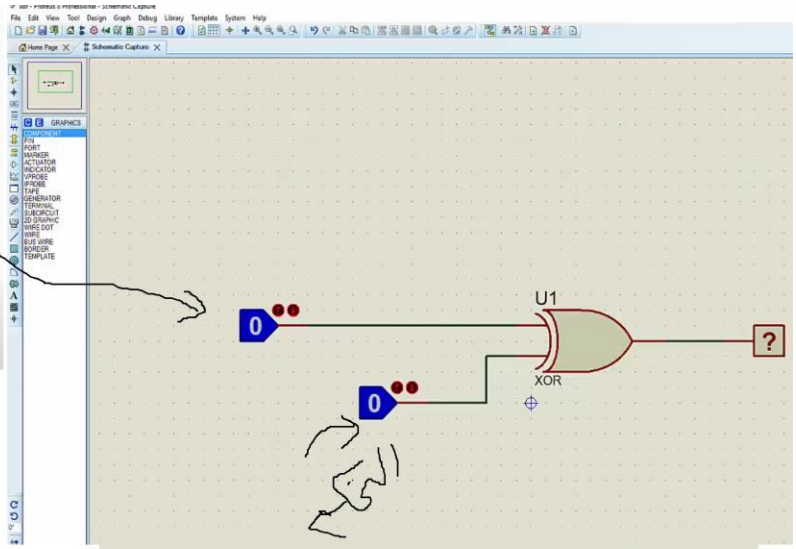


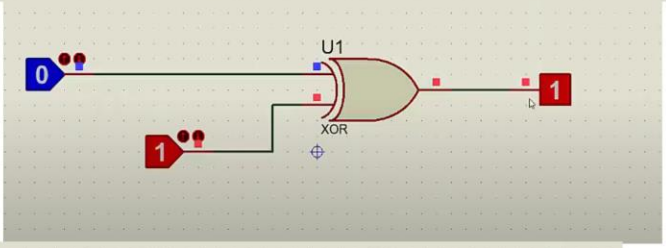


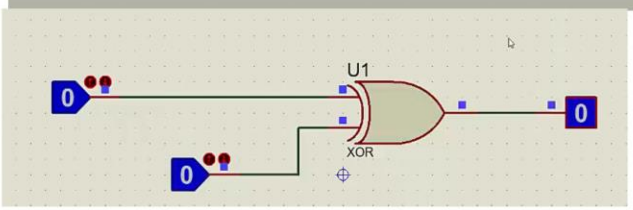


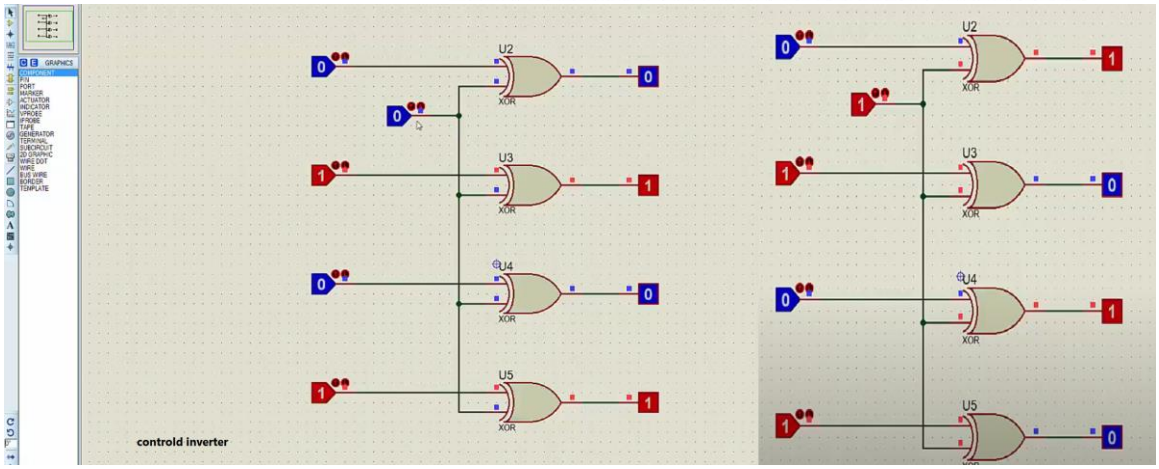
التطبيقات

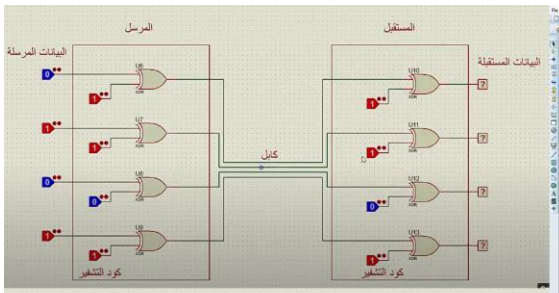
- جمع وطرح الاعداد
- المقارنة واكتشاف الاختلاف
- عكس الارقام
- التشفير

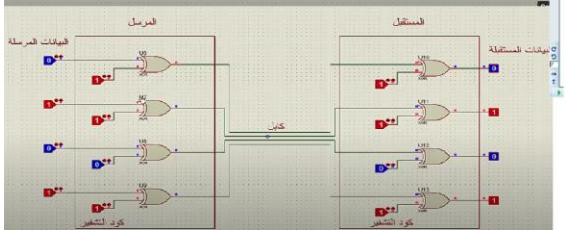


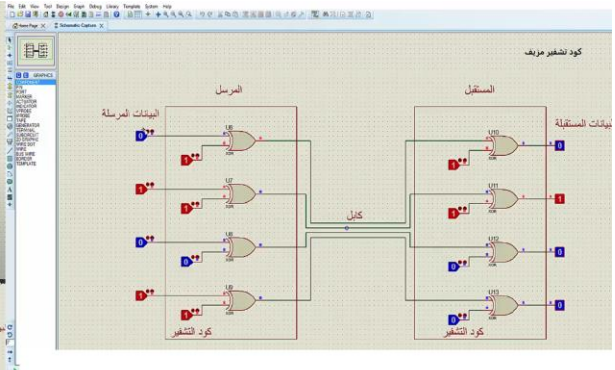







المرسل
المستقبل
البيانات المرسلة
البيانات المستقبلة
كابل
كود التشفير
كود التشفير

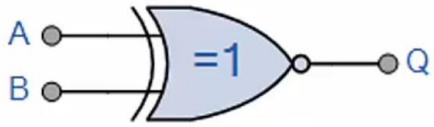

المرسل
المستقبل
البيانات المرسلة
بيانات المستقبلة
كابل
كود التشفير
كود التشفير


كود تشفير مزيف
المرسل
المستقبل
البيانات المرسلة
كابل
كود التشفير
كود التشفير

بوابة XNOR Exclusive NOR بوابة

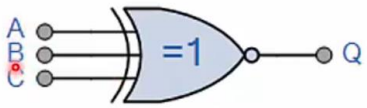
بوابة التكافؤ

2-input "Ex-OR" gate plus a "NOT" gate

Symbol	Truth Table		
	B	A	Q
	0	0	1
	0	1	0
	1	0	0
	1	1	1
Boolean Expression $Q = \overline{A \oplus B}$	Read if A **AND** B the **SAME** gives Q		

2-input Ex-NOR Gate

ذات ثلاث مداخل

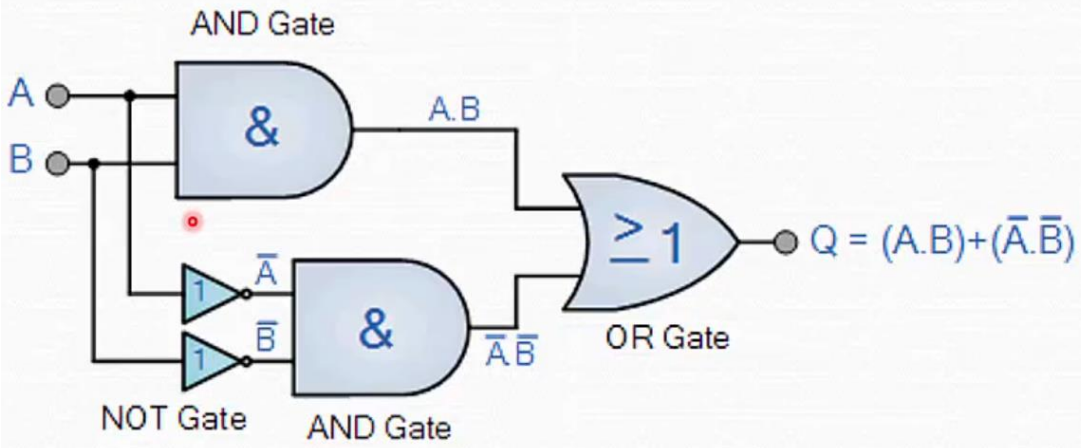
Symbol	Truth Table			
	C	B	A	Q
	0	0	0	1
	0	0	1	0
	0	1	0	0
	0	1	1	1
	1	0	0	0
	1	0	1	1
	1	1	0	1
	1	1	1	0
Boolean Expression $Q = \overline{A \oplus B \oplus C}$	Read as "any **EVEN** number of Inputs" gives Q			

3-input Ex-NOR Gate

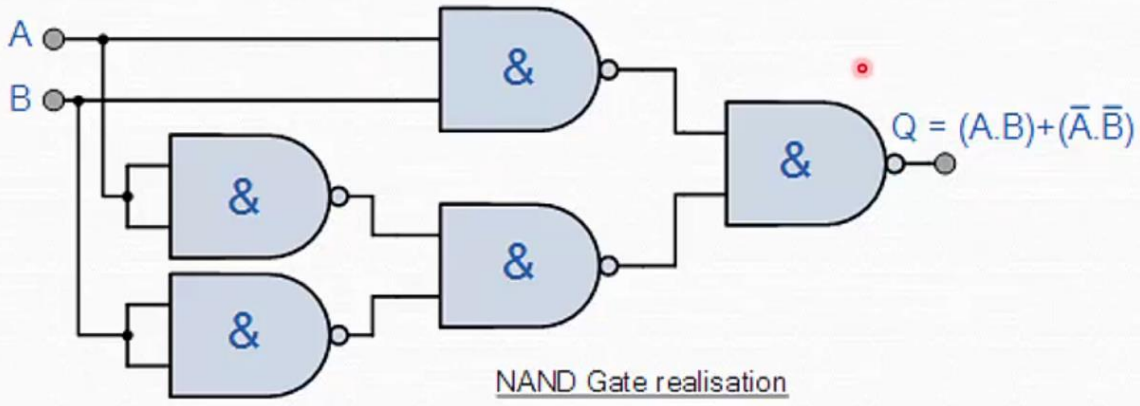
يكون الخرج 1 عندما يكون هناك عدد زوجي من المداخل 1 ... والعدد الزوجي يشمل الصفر

ملاحظة اذا كان هناك مدخل زائد عن الحاجة يجب ربطه بـ **0** فولت (**Logic 0**)
هنا خطأ كبير لو تم ربطه بمدخل آخر (أي دمج مدخلين مع بعض)

XNOR من البوابات الرئيسية

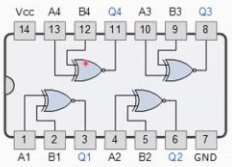


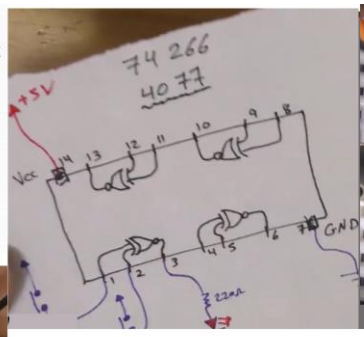
XNOR من بوابة NAND

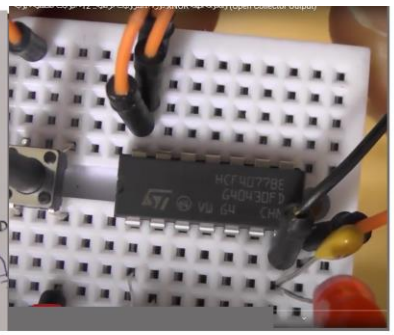


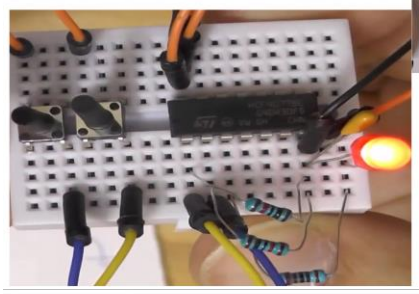
TTL Logic Types
74LS266 Quad 2-input

CMOS Logic Types
CD4077 Quad 2-input









FAIRCHILD SEMICONDUCTOR

March 1989
Revised March 2000

DM74LS266 Quad 2-Input Exclusive-NOR Gate

DM74LS266
Quad 2-Input Exclusive-NOR Gate with Open-Collector Outputs

General Description

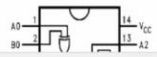
This device contains four independent gates each of which performs the logic exclusive-NOR function. Outputs are open collector.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS266M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS266N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Truth Table

Inputs		Outputs
A	B	Y
L	L	H

TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS055E

January 1998 - Revised September 2003

CD4070B, CD4077B
CMOS Quad Exclusive-OR and Exclusive-NOR Gate

Features

- High-Voltage Types (20V Rating)
- CD4070B - Quad Exclusive-OR Gate
- CD4077B - Quad Exclusive-NOR Gate
- Medium Speed Operation
  - t_{PHL}, t_{PLH} = 65ns (Typ) at V_{DD} = 10V, C_L = 50pF
- 100% Tested for Quiescent Current at 20V
- Standardized Symmetrical Output Characteristics
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1µA at 18V Over Full Package Temperature Range
  - 100nA at 18V and 25°C
- Noise Margin (Over Full Package Temperature Range)
  - 1V at V_{DD} = 5V, 2V at V_{DD} = 10V, 2.5V at V_{DD} = 15V
- Meets All Requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices

Applications

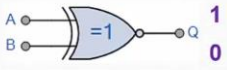
- Logical Comparators

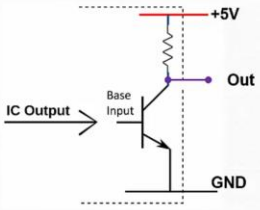
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD4070BE	-55 to 125	14 Ld PDIP
CD4070BF3A	-55 to 125	14 Ld CERDIP
CD4070BM	-55 to 125	14 Ld SOIC
CD4070BMT	-55 to 125	14 Ld SOIC
CD4070BM96	-55 to 125	14 Ld SOIC
CD4070BNSR	-55 to 125	14 Ld SOP
CD4070BPW	-55 to 125	14 Ld TSSOP
CD4070BPWR	-55 to 125	14 Ld TSSOP
CD4077BE	-55 to 125	14 Ld PDIP
CD4077BF3A	-55 to 125	14 Ld CERDIP
CD4077BM	-55 to 125	14 Ld SOIC
CD4077BMT	-55 to 125	14 Ld SOIC
CD4077BM96	-55 to 125	14 Ld SOIC

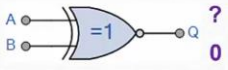
Open Collector / Open Drain الخرج من نوع

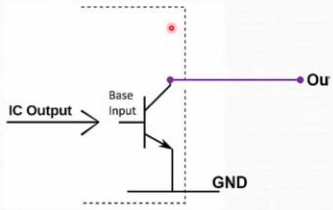
الوضع العادي



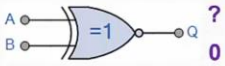


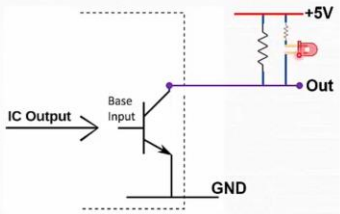
وضع الـ open

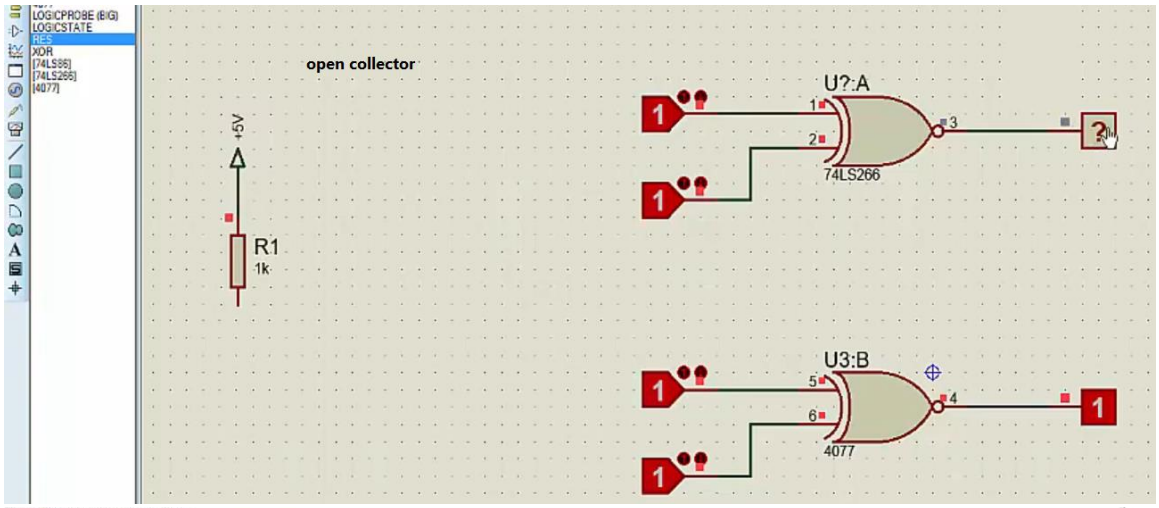


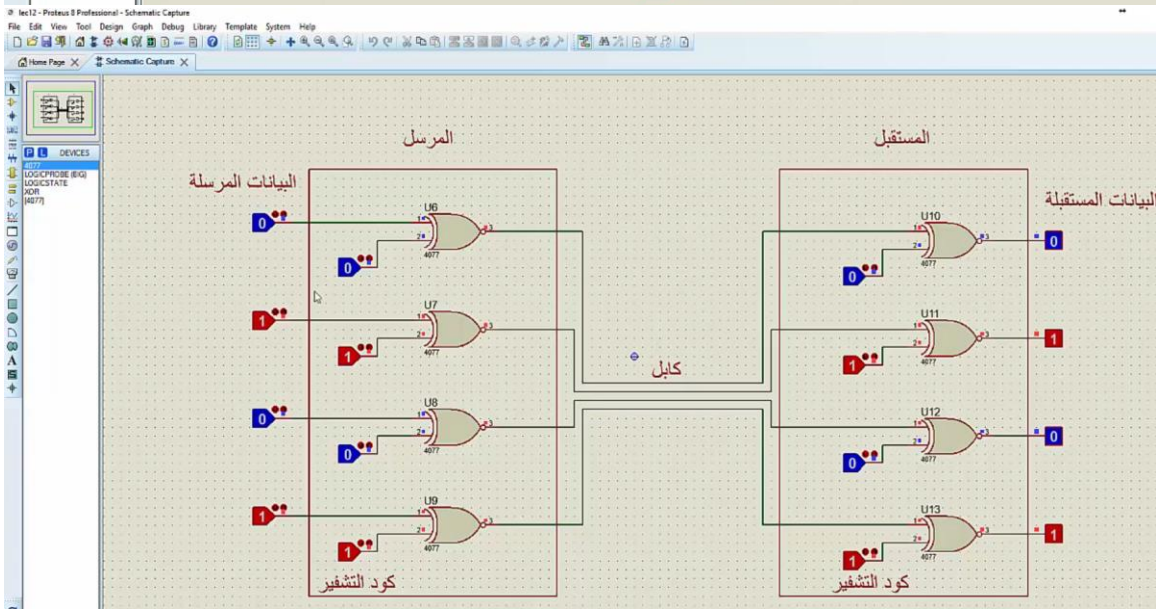


وضع الـ open






LOGICPROBE (BIG)
LOGICSTATE
RES
XOR
[74LS86]
[74LS266]
[4077]
open collector
+5V
R1
1k
U?:A
74LS266
U3:B
4077


lec12 - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Home Page
Schematic Capture
DEVICES
LOGICPROBE (BIG)
LOGICSTATE
XOR
[4077]
المرسل
المستقبل
البيانات المرسلة
البيانات المستقبلة
كابل
كود التشفير
كود التشفير
U6
U7
U8
U9
U10
U11
U12
U13
4077